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Semiconductor Measurement Technology:

Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon

00-22

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PREFACE

The work was conducted as part of the Semiconductor Technology Program at the National Bureau of Standards. Portions of this work were supported by the Defense Nuclear Agency (IACRO 75-816), Defense Advanced Research Projects Agency (Order No. 2397), U.S. Navy Strategic Systems Project Office (IPR SP-75-4), and the NBS.

In the semiconductor industry it is common practice to design photomasks in English units. The photomasks used in this study were laid out in English units. The equivalent metric unit is given in parentheses; in some cases the equivalent is rounded off to an appropriate number of significant figures.

MICROELECTRONIC TEST PATTERN NBS-3 FOR EVALUATING THE RESISTIVITY-DOPANT DENSITY RELATIONSHIP OF SILICON

by

Martin G. Buehler

Abstract: Test pattern NBS-3 is a microelectronic test vehicle designed by the National Bureau of Standards to evaluate the electronic materials used in discrete semiconductor devices and integrated circuits. Designed for fabrication on silicon wafers, the test pattern is an aid in better understanding integrated circuit fabrication technologies. The main pattern consists of four masks designated BASE, EMITTER, CONTACT, and METAL and contains 33 test structures such as sheet resistors, MOS capacitors, *p*-*n* junctions, bipolar and MOS transistors, and etch control and resolution structures.

The pattern was designed primarily to aid in the evaluation of the relationship between resistivity and dopant density in both *n*- and *p*-type silicon. This relation is needed in the design of silicon solid-state devices and in the analysis of various physical measurements. Other test structures are included for use as diagnostic tools to verify that proper fabrication procedures were followed. The remaining structures allow the exploration of new designs and measurement methods.

The structures are arranged in a square pattern 200 mil (5.08 mm) on a side. A detailed layout of each test structure is presented including both a top view and a cross sectional view. A description of each structure is given and where applicable the formulas for evaluating such quantities as resistivity, dopant density, and sheet resistance are given. The fabrication of the test pattern is illustrated by an *n*-*p*-*n* transistor process and values obtained from various test structures are presented.

Key Words: Dopant density; microelectronics; MOS capacitors; *n*-*p*-*n* transistor fabrication; *p*-*n* junctions; resistivity; semiconductor electronics; sheet resistors; silicon; test pattern; test structures.

1. INTRODUCTION

This test pattern follows in a series of microelectronic test patterns intended for use in the design, process control, and product assurance of discrete devices and integrated circuits. The use of these patterns by manufacturers is expected to lead to lower cost and more reliable electronic components. When fully developed, they are intended to be utilized by the buyers of microelectronic components in purchase specifications. The previous pattern, NBS-2 [1], was designed so that we could fabricate various test structures needed for the development of various measurement methods. Test pattern NBS-3 was designed primarily to evaluate the resistivity versus dopant density relation in *n*- and *p*-type silicon. Other secondary purposes include the evaluation of test structures for use as process control tools and the development of new and improved test structures. The purpose of this report is to describe the test structures found on test pattern NBS-3, to indicate the test methods associated with the dopant density and resistivity

measurements, and to present selected test structure results from a wafer fabricated with an *n*-*p*-*n* transistor process.

The resistivity-dopant density relation for silicon is commonly taken from the experimental data of Irvin [2]. Caughey and Thomas [3] have written closed-form mathematical formulas which fit the Irvin data for both *n*- and *p*-type silicon. Recently, Wagner [4] has indicated that the *p*-type relation is in error by about 50 percent for dopant density near 10^{18} cm^{-3}. NBS has undertaken to reevaluate the resistivity-dopant density relation at the request of and in conjunction with ASTM Committee F-1 on Electronics. The main test vehicles are silicon wafers on which test pattern NBS-3 is fabricated. Preliminary results of our investigation are presented elsewhere [5].

The test structures found on test pattern NBS-3 are listed in table 1. The overall pattern, shown in figure 1, is fabricated on a square silicon chip 200 mil (5.08 mm) on a side where four mask levels were used. Enlarged views of the test pattern are shown in the Appendix. Four different masks were designed and are intended to be used in the following sequence: BASE, EMITTER, CONTACT, and METAL. Provision was made in the design to allow for the incorporation of a fifth PASSIVATION mask. The BASE mask delineates regions whose conductivity type is opposite from the collector substrate, and the EMITTER mask delineates regions whose conductivity type is the same as the collector substrate.

A BASE (modified) mask was designed to address a special problem with structures 3.12, 3.17, and 3.18. These structures have small collector contacts which are formed by blocking the large-area base diffusion at the contact points. This allows the formation of a collector pipe which reaches through to the top silicon surface. In order to block the base diffusion at a contact point, a base-oxide island is formed which is a square 0.25 mil (6.4 μm) on a side. During fabrication, the base-oxide island is over-etched by 0.10 mil (2.5 μm) which reduces the oxide island to a square 0.15 mil (3.8 μm) on a side. This means that the base lateral diffusion must be less than 1.9 μm to prevent the closing off of the collector pipe. To reduce this problem, a BASE (modified) mask was designed where the 41 square base-oxide islands, found on structures 3.12, 3.17, and 3.18, were increased to 0.50 mil (12.7 μm) on a side. When the BASE (modified) mask is used, the lateral diffusion can be as large as 5.1 μm assuming that the base-oxide is over-etched by 0.10 mil (2.5 μm).

The chip is composed of an array of 33 test structures such as sheet resistors, MOS capacitors, *p*-*n* junctions, bipolar and MOS transistors, and etch control and resolution structures which for the most part are adaptations of commonly used configurations. It should be noted that the collector Hall effect resistor (3.26) is functional only after it has been scribed from the wafer and the backside metal removed. To accommodate this structure, the scribe grid was omitted from the BASE and EMITTER masks and included on only the CONTACT mask.

Structures specifically designed for the resistivity-dopant density evaluation are indicated by asterisks in table 1. Bulk collector dopant density values can be determined from the following structures: MOS capacitor over collector (3.8), base-collector diode (3.10), and collector Hall effect resistor (3.26). In obtaining dopant density values from the MOS capacitor over collector, the high frequency C-V deep depletion method [6] provides true bulk values. The high frequency C-V C_{max}-C_{min} method [7] can give erroneous values since this method is influenced by the redistribution of impurities at the oxide-silicon interface during the oxidation process [7]. Values obtained from the collector Hall effect resistor (3.26) rely on a knowledge of the scattering factor [8], [9] which is not well established in *p*-type silicon [8]. Dopant density values can be obtained from the base-collector diode (3.10) by using the junction C-V method [10].

Bulk resistivity values can be found from the collector resistors (3.1, 3.7, 3.12, 3.17, and 3.18) and the collector Hall effect resistor (3.26). Collector

resistors (3.1, 3.7, 3.12, and 3.18) are intended to operate with current passing from the top of the chip to the backside contact. In this mode, backside contact resistance and geometrical factors must be determined. Collector resistors 3.12 and 3.18 yield information about the backside contact resistance, and collector resistor (3.7) was designed to have a readily calculable geometrical factor. The collector four-probe resistor (3.17) is a conceptually simple structure, but it requires the fabrication of a bipolar transistor. This device is easy to measure and provides unambiguous bulk resistivity values which do not depend on a knowledge of the backside contact resistance. The collector Hall effect resistor (3.26) can yield unambiguous resistivity values but, as noted above, it requires that wafers be scribed into chips and the removal of the backside metallization.

Resistivity and dopant density values can be obtained continuously from base profiles by combining the results of two test structures. The base dopant density profiles can be obtained from the emitter-base diode (3.9) with use of the junction C-V, method and the base resistivity profile can be obtained from the tetrode transistor (3.6). With the use of methods described elsewhere [11], these two structures allow resistivity values to be determined over several decades in dopant density.

Many of the remaining test structures are in support of the above structures. They are intended to assure that proper fabrication steps were followed and to aid in diagnosing problems.

2. DESIGN

In designing the test structures for test pattern NBS-3 the following design rules were observed:

1. Minimum stripe width: 0.25 mil (6.4 μm).
2. Minimum base to channel stop separation: 0.50 mil (12.7 μm).
3. Minimum emitter to base separation: 0.50 mil (12.7 μm).
4. Minimum contact to base (or emitter) separation: 0.50 mil (12.7 μm).
5. Metal overlap at contacts: 0.25 mil (6.4 μm) [0.50 mil (12.7 μm) where a passivation layer is opened].
6. Minimum field plate overlap at diffusions: 0.50 mil (12.7 μm).
7. Minimum metal separation: 0.50 mil (12.7 μm).
8. Exposed bonding pad width when a passivation layer is used: 4.00 mil (101.6 μm).
9. Minimum passivation overlap at metal: 0.25 mil (6.4 μm).
10. Scribe grid width: 4.00 mil (101.6 μm).
11. Expanded metallization contacts: avoided where possible by extending diffusions under contacts.
12. Top side contacts: provided whenever possible.
13. The lines on each mask level: uniquely located so that they do not coincide with the lines on another mask level.

These rules were chosen to minimize problems encountered in pinhole shorting, mask aligning, probing, bonding, and inspecting. For instance, a misalignment of ± 0.25 mil (6.4 μm) between the CONTACT and METAL masks and between the CONTACT and BASE masks is tolerable. Eliminating expanded metal contacts reduces pinhole shorting problems associated with contacts. Unique location of lines on each mask level simplifies inspection procedures. These design rules eliminate certain fabrication faults and thereby improve the chances that a test structure will function properly.

Table 1 - Planar Test Structures on Test Pattern NBS-3

Page Number	Section Number	Structure Number	Test Structure[a]
15	4.11	3.1	*Collector resistor (FP, CS)
23	5.4	3.2	MOS capacitor over base
24	5.5	3.3	MOS capacitor over emitter
34	8.4	3.4 N, P	Alignment markers
34	8.5	3.5	NBS logo
28	7.2	3.6	*Tetrode transistor
18	4.14	3.7	*Collector resistor (DGR)
21	5.1	3.8	*MOS capacitor over collector (FP, CS)
27	6.3	3.9	*Emitter-base diode (FP)
25	6.1	3.10	*Base-collector diode (FP, CS)
9	4.3	3.11	Base sheet resistor (VDP, FP, CS)
16	4.12	3.12	*Collector spreading resistor (small)
28	7.1	3.13	Bipolar transistor
26	6.2	3.14	Base-collector diode (FP, CS)
31	7.4	3.15	MOS transistor (circular)
30	7.3	3.16	MOS transistor
19	4.15	3.17	*Collector four-probe resistor
17	4.13	3.18	*Collector spreading resistor (large)
22	5.2	3.19	MOS capacitor over collector
12	4.7	3.20	Metal sheet resistor (VDP)
11	4.5	3.21	Emitter sheet resistor (VDP)
7	4.1	3.22	Base sheet resistor (VDP)
14	4.9	3.23	Metal-to-emitter contact resistor
13	4.8	3.24	Metal-to-base contact resistor
22	5.3	3.25	MOS capacitor over collector
20	4.16	3.26	*Collector Hall effect resistor
11	4.6	3.27	Emitter sheet resistor (B)
8	4.2	3.28	Base sheet resistor (B)
32	8.1	3.29	Surface profile structure
10	4.4	3.30	Incremental base sheet resistor (VDP)
33	8.2	3.31 B, E, C, M	Etch-control structures[b]
34	8.3	3.32 B, C, M	Resolution structures[b]
14	4.10	3.33	Metal step-coverage resistor

[a] B = bridge; CS = channel stop; DGR = diffused guard; FP = field plate; N = negative photoresist; P = positive photoresist; VDP = van der Pauw.

[b] B = BASE mask; E = EMITTER mask; C = CONTACT mask; M = METAL mask.

* Structures designed for the resistivity-dopant density evaluation.

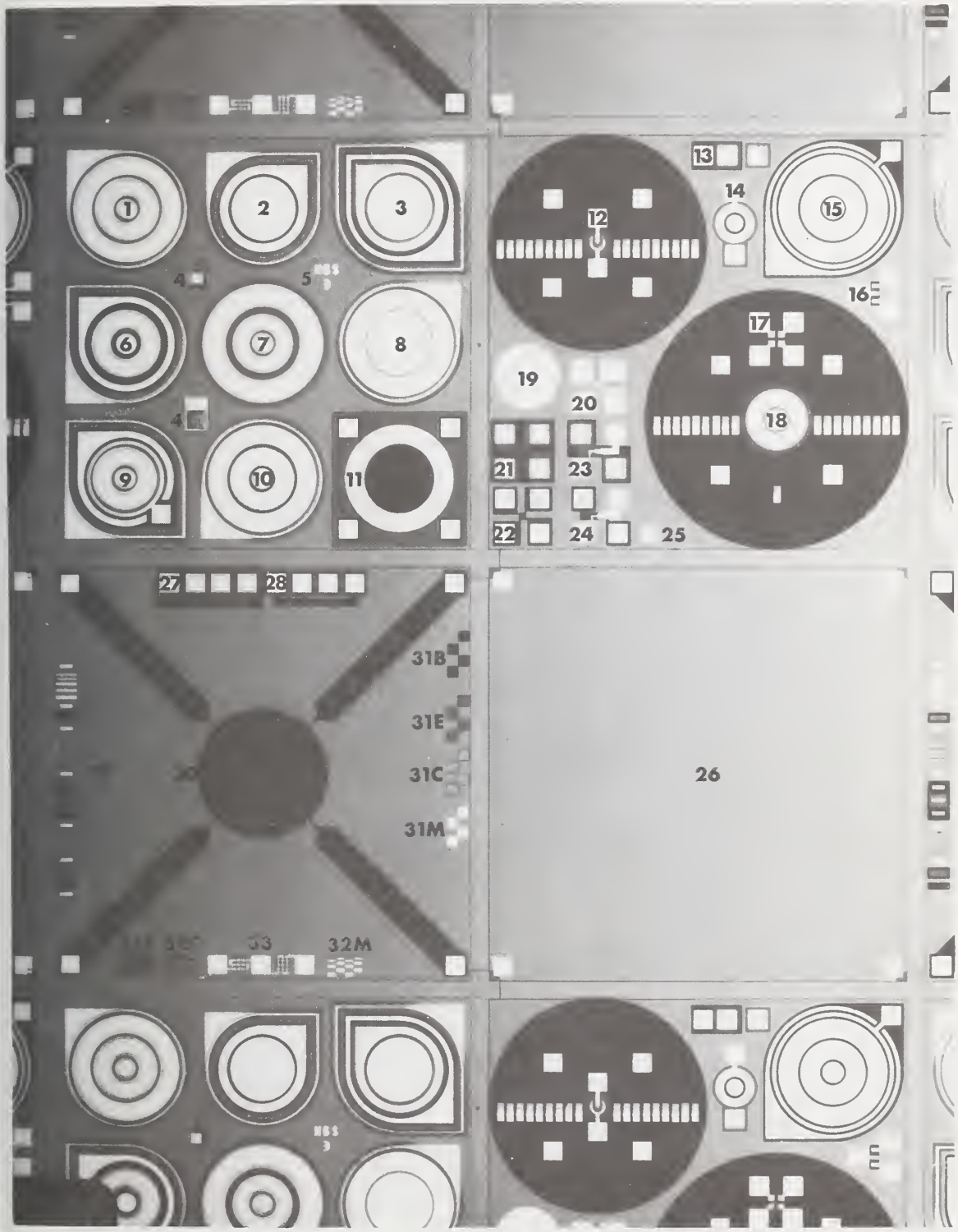


Figure 1. Test pattern NBS-3 fabricated with the BASE (B), EMITTER (E), CONTACT (C), and METAL (M) masks. The length of the pattern along one side is 200 mil (5.08 mm).

3. TEST STRUCTURES

In sections 4 through 8 each test structure is described along with the intended purpose. The structures are grouped in five major categories: resistors, MOS capacitors, diodes, transistors, and miscellaneous. Formulas for calculating such quantities as resistivity, dopant density, and sheet resistance are presented where applicable. The symbols used in the following text are explained at the bottom of table 1 or are indicated on the relevant test structure.

In the following sections both a detailed top view layout and cross sectional view of each test structure are given. Figure 2 illustrates the scheme used. In the top views the distance between grid lines represents 0.50 mil (12.7 μm). In the cross sectional views, metal regions are black and oxide regions are dotted. Emitter regions are clear and indicated by a solid line one unit below the silicon surface. Base regions are clear and indicated by a solid line two units below the silicon surface. (In these views a *unit* is the distance between adjacent grid lines. Also the silicon surface is assumed to be flat for the sake of simplicity; the incorporation of silicon into the oxide during thermal oxidation has been ignored.)

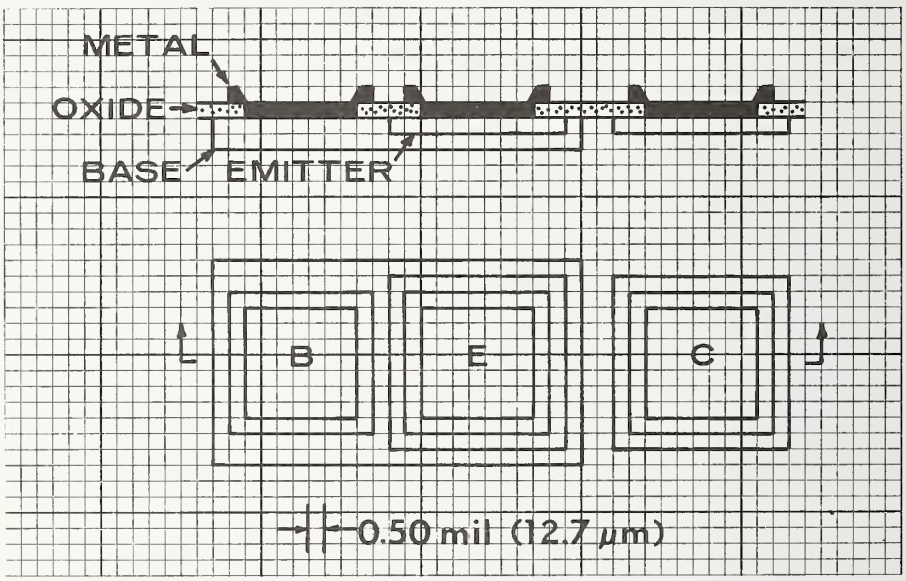


Figure 2. An illustration of the notation used in the cross sectional view of a test structure. The distance between grid lines is 0.50 mil (12.7 μm). In the top view B = base, E = emitter, and C = collector.

In the text the term *emitter* applies to both bipolar transistor emitter regions and to channel stop (CS) regions. The term *base* applies to both bipolar transistor base regions and to MOS transistor source-drain regions. Emitter and collector refer to regions with the same conductivity type which is opposite from the conductivity of base regions. The emitter is more heavily doped than the collector.

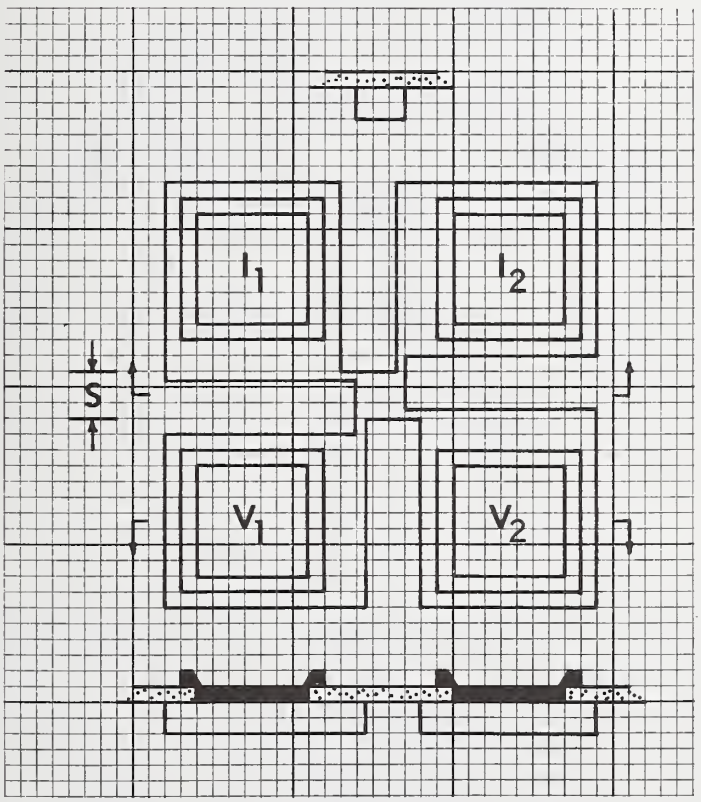
4. RESISTORS

4.1. Base Sheet Resistor (VDP), Structure 3.22

Base sheet resistor (VDP), structure 3.22, is a four-terminal resistor arranged in an orthogonal van der Pauw (VDP) configuration [12] and consists of a base diffused into the collector. As indicated below the active base region is a square whose side, S, is 1.50 mil (38.1 μm) which is typical of integrated circuit device geometries. The sheet resistance, R_s(VDP), is calculated from

$$R_s(\text{VDP}) = (V/I)(\pi/\ln 2) \qquad (1)$$

where the potential, V, is V_1-V_2 for a current, I, passed into I_1 and out of I_2.



4.2. Base Sheet Resistor (B), Structure 3.28

Base sheet resistor (B), structure 3.28, is a four-terminal resistor arranged in a bridge (B) configuration and consists of a base diffused into the collector. This structure was designed according to ASTM standard F 76 [13]. The photomask dimension for the oxide window width, W(mask), is 1.50 mil (38.1 μm and the length, L(mask), between voltage taps is 6.0 mil (152 μm). The sheet resistance, R_s, is calculated from

$$R_s = (V/I)[W_e/L(mask)] \tag{2}$$

where the potential, V, is V_1-V_2 for a current, I, passed into I_1 and out of I_2. The effective window width, W_e, is

$$W_e = W(mask) + \alpha X_j + W_{oe} \tag{3}$$

where X_j is the junction depth, α is a coefficient which accounts for lateral diffusion effects [14], W_{oe} is the over-etch width. These quantities are illustrated in figure 3. Combination of the I/V ratio measured from this

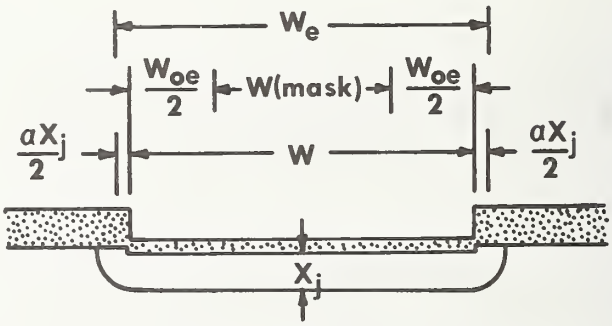
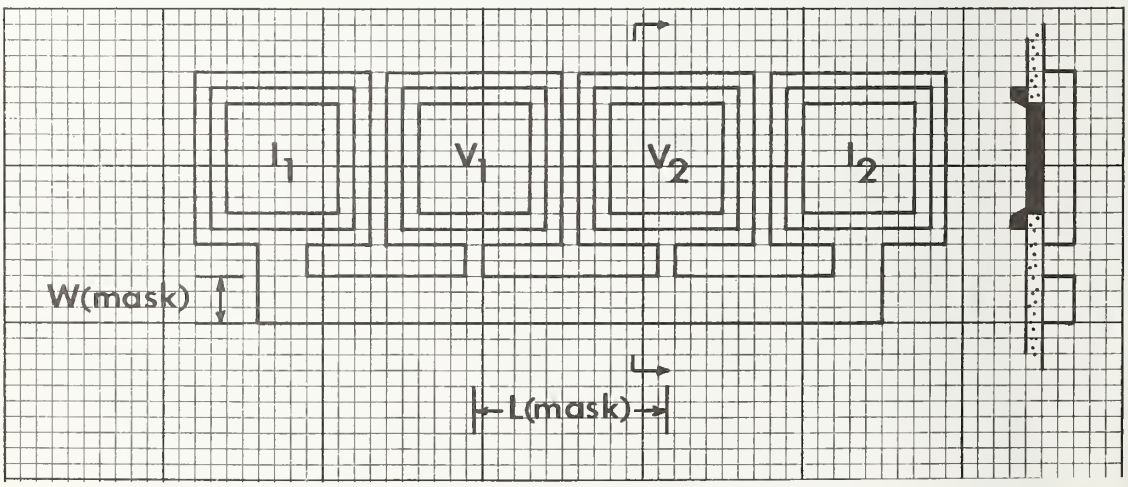


Figure 3. Cross sectional view of a diffused region showing various dimensions.

structure with the sheet resistance R_s(VDP) measured from structure 3.22 leads to an equation for the effective base window width, W_e, [15]:

$$W_e = R_s(VDP)L(mask)(I/V). \tag{4}$$

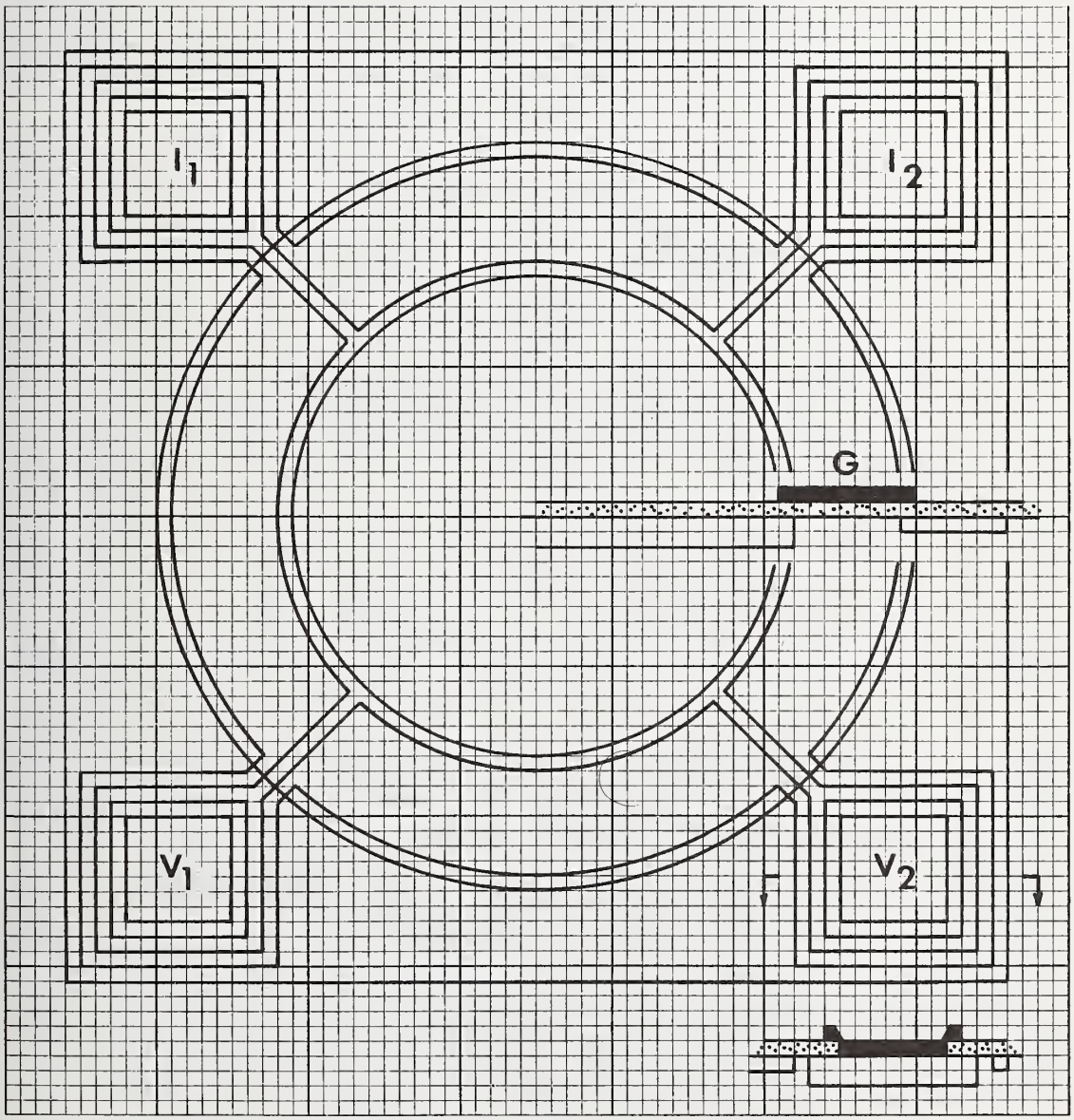


4.3. Base Sheet Resistor (VDP, FP, CS), Structure 3.11

Base sheet resistor (VDP, FP, CS), structure 3.11, is a four-terminal resistor arranged in a van der Pauw (VDP) configuration [12] and consists of a base diffused into the collector. An emitter is diffused around the base and acts as a channel stop (CS). A metal field plate (FP) lies on top of the collector oxide between the base and channel stop and serves to shut off surface currents when it is biased so as to accumulate the collector. The active region is a circle 17.0 mil (432 μm) in diameter. The sheet resistance, R_s, is calculated from

$$R_s = (V/I)(\pi/\ell n 2) \tag{5}$$

where the potential, V, is V_1-V_2 for a current, I, passed into I_1 and out of I_2. This structure is useful when evaluating sheet resistances greater than 1000 Ω/□.



4.4. Incremental Base Sheet Resistor (VDP), Structure 3.30

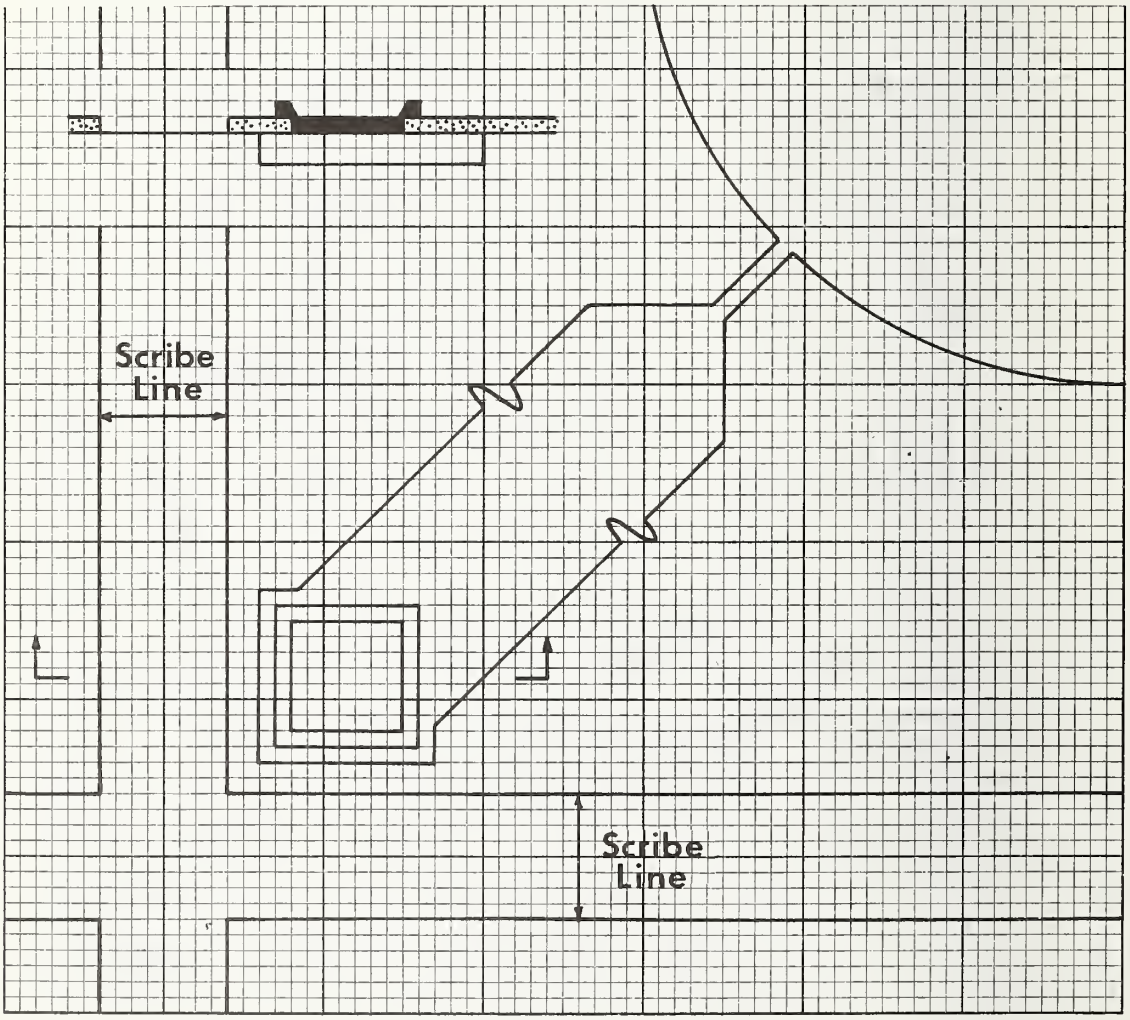
Incremental base sheet resistor (VDP) structure 3.30, is a four-terminal resistor arranged in a van der Pauw (VDP) configuration [12] and consists of a base diffused into the collector. The active region is 30.0 mil (762 μm) in diameter. The sheet resistance, R_S, is calculated from

$$R_S = (V/I)(\pi/\ln 2) \tag{6}$$

where the potential, V, and the current, I, are measured at the ends of the four legs. This structure was designed to facilitate the measurement of dopant profiles by the incremental sheet resistance method [16]. The resistivity, ρ_i, of the increment is

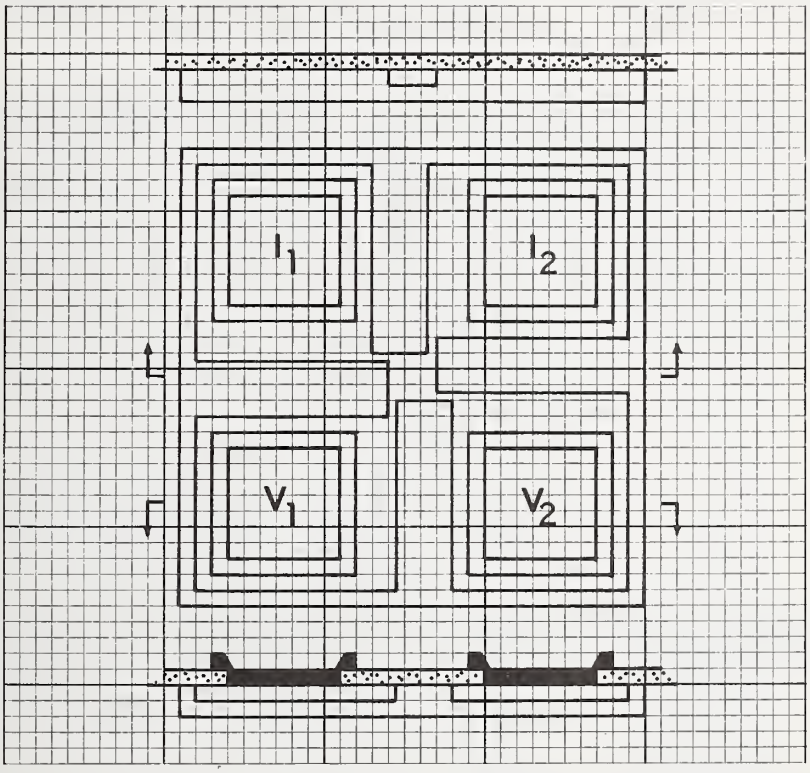
$$\rho_i^{-1} = \Delta R_S^{-1}/\Delta X \tag{7}$$

where ΔX is the thickness of the increment and ΔR_S is the sheet resistance of the increment. This method requires a method for determining ΔX and, in order to obtain dopant density values, requires a knowledge of the resistivity dopant density relation. An apparatus for automating this measurement is described elsewhere [17].



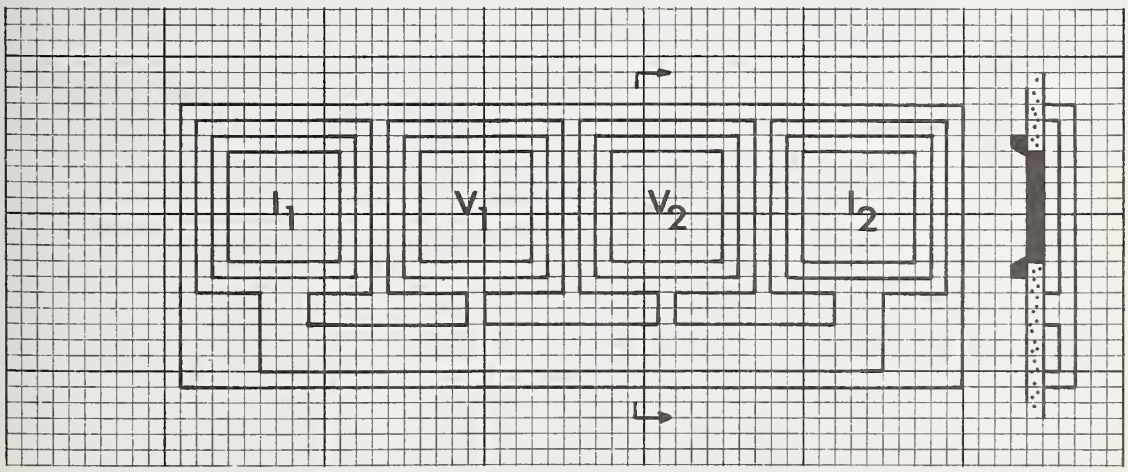
4.5. Emitter Sheet Resistor (VDP), Structure 3.21

Emitter sheet resistor (VDP), structure 3.21, is a four-terminal resistor arranged in an orthogonal van der Pauw (VDP) configuration [12] and consists of an emitter diffused into a base. The discussion for structure 3.22, section 4.1, is applicable to structure 3.21.



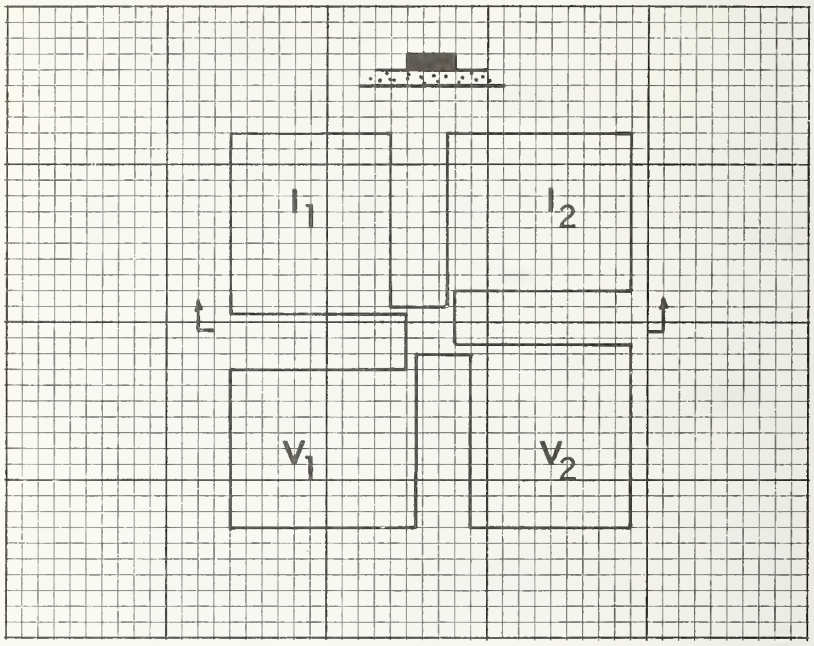
4.6 Emitter Sheet Resistor (B), Structure 3.27

Emitter sheet resistor (B), structure 3.27, is a four-terminal resistor arranged in a bridge (B) configuration and consists of an emitter diffused into a base. The discussion for structure 3.28, section 4.2, is applicable to structure 3.27.



4.7. Metal Sheet Resistor (VDP), Structure 3.20

Metal sheet resistor (VDP), structure 3.20, is a four-terminal resistor arranged in a van der Pauw (VDP) configuration [12] and consists of metal deposited over the collector oxide. The discussion for structure 3.22, section 4.1, is applicable to structure 3.20. The arms on this structure have a width of 0.25 mil (6.4 μm) which requires tight control of the metal etch step to prevent the arms from being etched away.

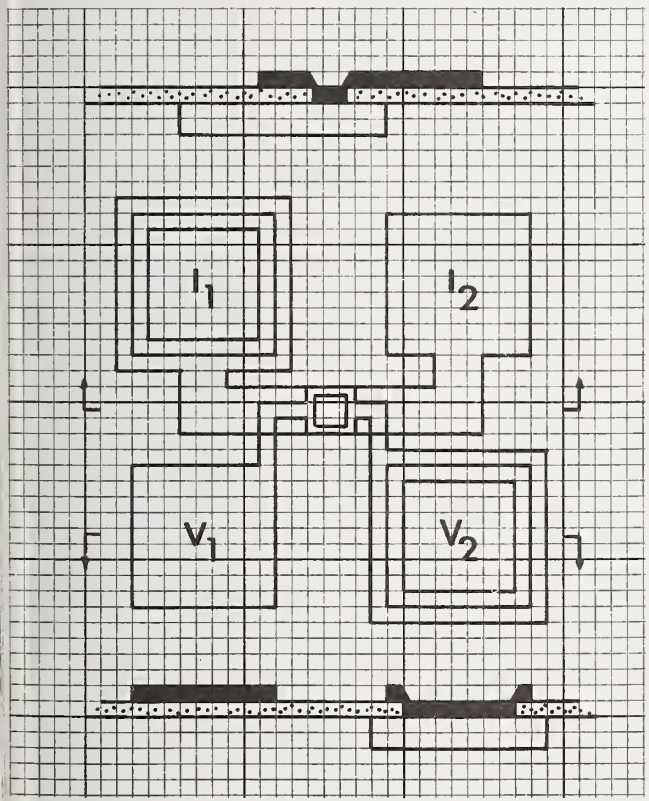


4.8. Metal-to-Base Contact Resistor, Structure 3.24

Metal-to-base contact resistor, structure 3.24, is a four-terminal resistor which consists of a base diffused into the collector and metal which touches the base at a square window 1.00 mil (25.4 μm) on a side; see figure 4. The effective contact resistance for a unit area, R_c, as given by this structure is calculated from

$$R_c = AV/I \tag{8}$$

where the potential, V, is V_1-V_2 for a current, I, passed into I_1 and out of I_2 and A is the area of the contact. For a square contact window of 1.00 mil (25.4 μm) on a side, $A = 6.45 \times 10^{-6}$ cm^{-2}. This structure is intended to serve as a process control monitor. It is not intended to yield absolute values for the specific contact resistance for the effective contact resistance determined by this structure is influenced by over-etch of the contact window and by current crowding effects since only a fraction of the contact carries a significant current [18]. Over-etch of a contact window occurs because the contact window is etched at the same time as the scribe lines. Etching the scribe lines requires removal of the collector oxide which is thicker than the base oxide.



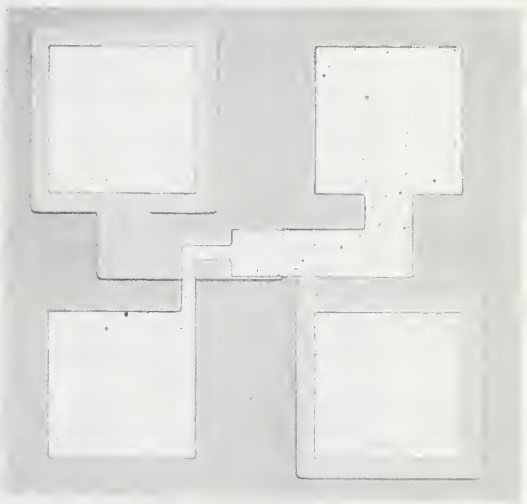
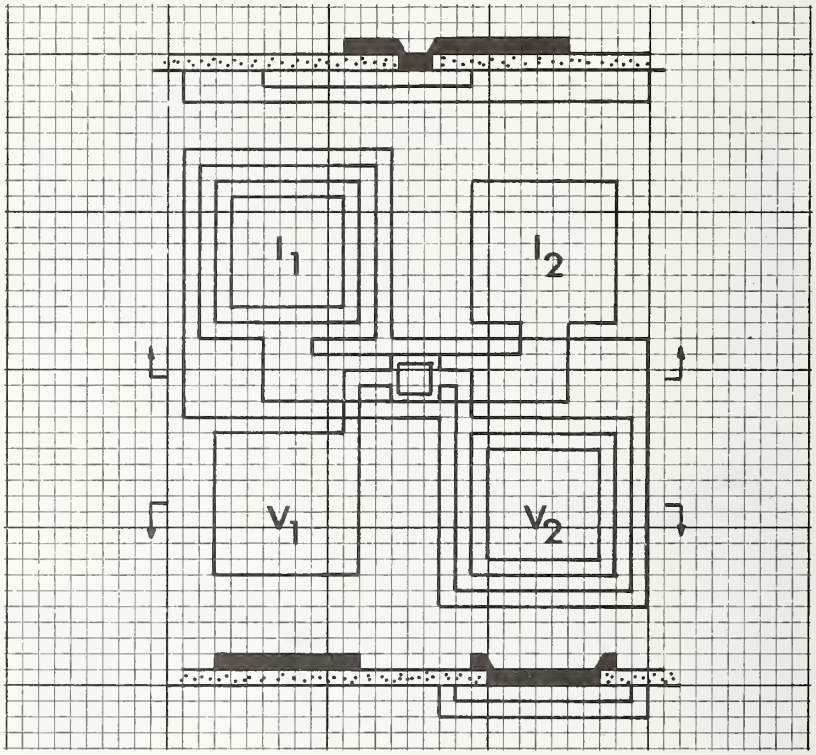


Figure 4. Photomicrograph of the metal-to-base contact resistor, structure 3.24.

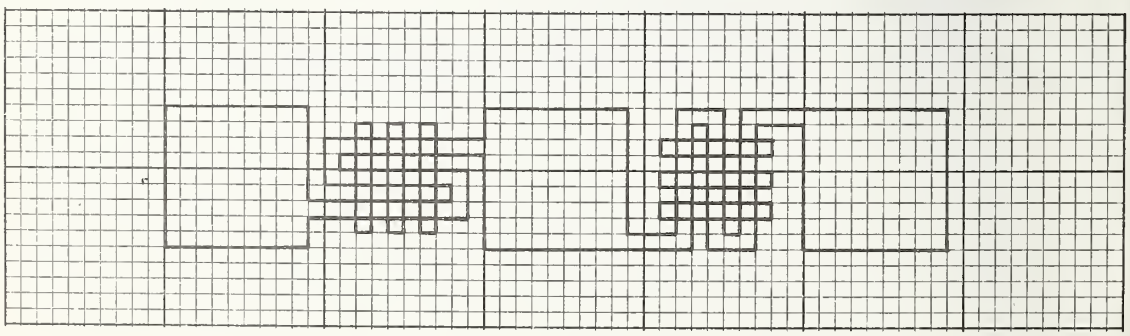
4.9. Metal-to-Emitter Contact Resistor, Structure 3.23

Metal-to-emitter contact resistor, structure 3.23, is a four-terminal resistor which consists of an emitter diffused into a base and metal which touches the emitter at a square window 1.00 mil (25.4 μm) on a side. The discussion for structure 3.24, section 4.8, is applicable to structure 3.23.



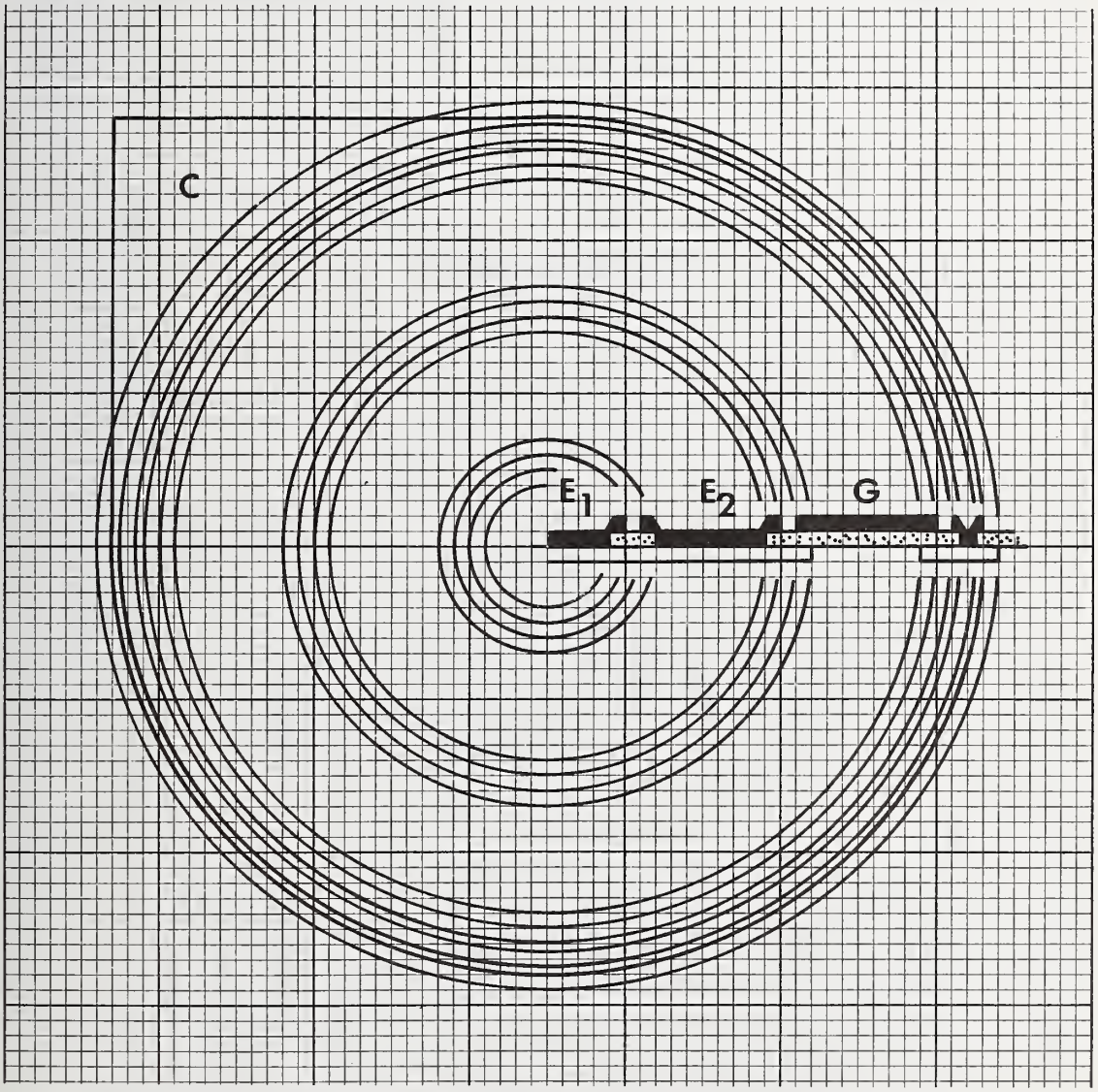
4.10 Metal Step-Coverage Resistor, Structure 3.33

Metal step-coverage resistor, structure 3.33, is a two-terminal resistor which consists of a serpentine metal path 0.50 mil (12.7 μm) wide which crosses 18 oxide steps etched by the CONTACT mask. Two resistors are combined into one structure. In one resistor the serpentine path crosses the oxide steps in a direction perpendicular to the other resistor. This allows a check of shadowing effects during metal deposition. This structure is used to check for metal continuity [19]. As shown below, the left-hand resistor is 31 squares long and the right-hand resistor is 35 squares long.



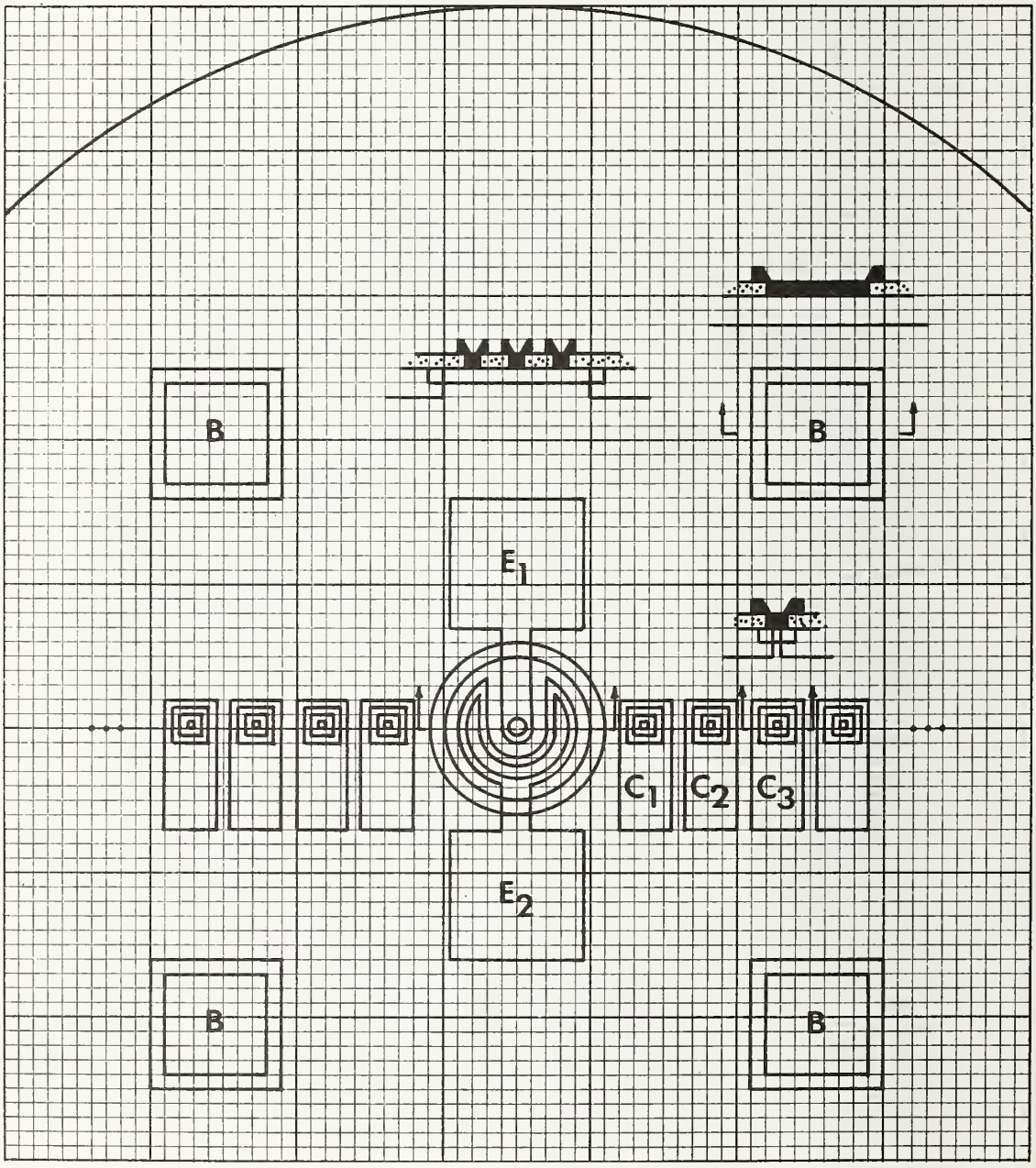
4.11. Collector Resistor (FP, CS), Structure 3.1

Collector resistor (FP, CS), structure 3.1, is a three-terminal resistor which consists of an emitter diffused into the collector. A metal field plate (FP) over the collector oxide controls the surface currents between the emitter and the channel stop (CS). The resistance is determined from the voltage drop between E_1 and the backside for a current between E_2 and the backside. In operation the field plate is biased so as to invert the collector surface. The collector resistivity is calculated with use of an expression which appropriately models the peripheral spreading resistance. Various expressions are available [20], [21]. This structure is intended for use on epitaxial layers deposited on more heavily doped substrates of the same conductivity type. The thickness of the layers must be small compared to the width of the field plate, 4.0 mil (102 μm), so that the peripheral current spreading is easily modeled. Since the backside contact resistance is in series with the collector, it must be negligibly small compared with the collector resistance in order to determine the collector resistivity accurately.



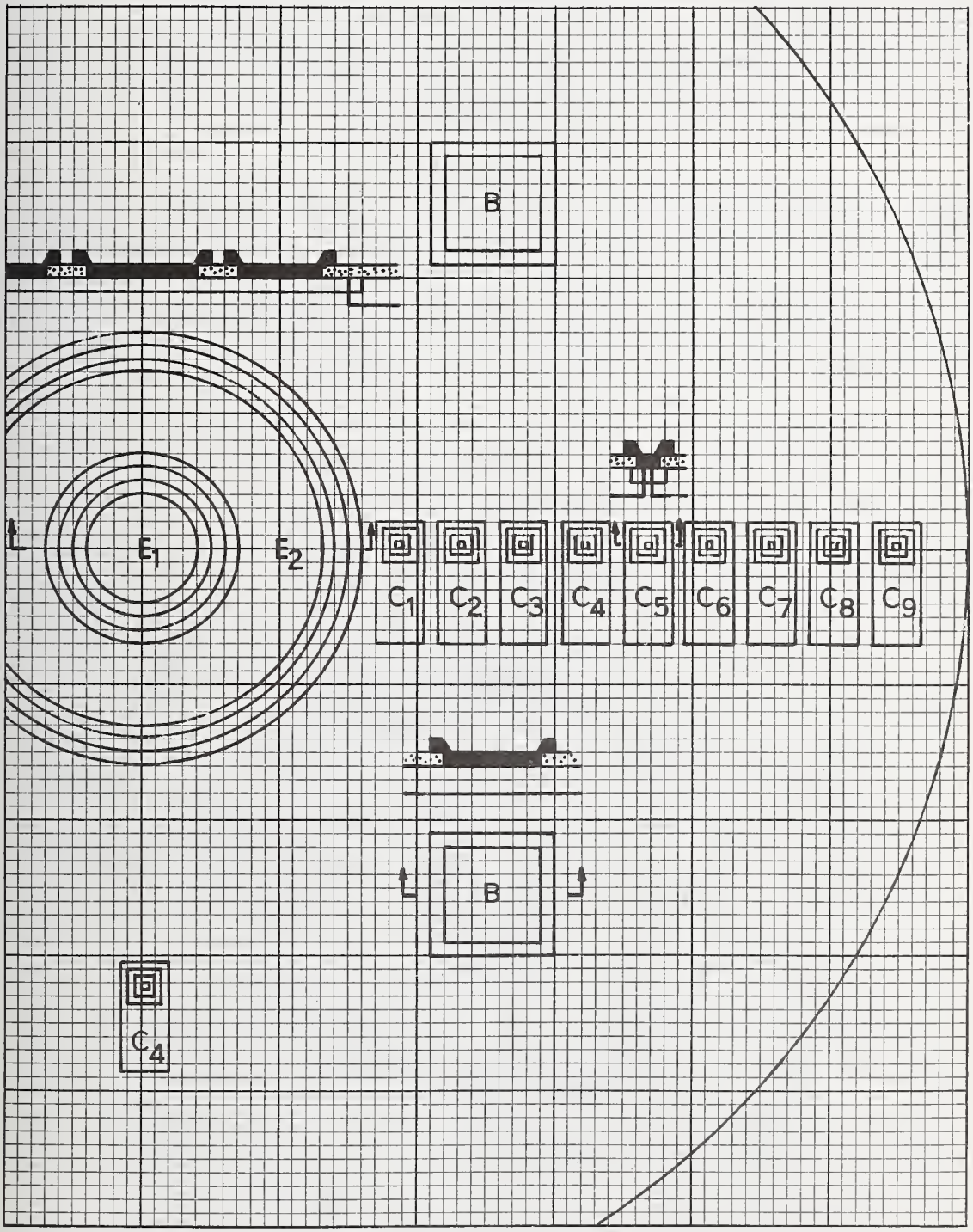
4.12. Collector Spreading Resistor (Small), Structure 3.12

Collector spreading resistor (small), structure 3.12, is a three-terminal resistor which consists of an emitter diffused into the collector. The emitter is surrounded by a base diffusion which eliminates surface currents. The base diffusion is broken at a series of points which serve as voltage taps to monitor the potential drop as a function of distance from the emitter. The drop in voltage with distance from the emitter is a sensitive monitor of the backside contact resistance. A linear model for this voltage drop is given by Bilotti [22] for the case of no contact resistance. In the absence of backside contact resistance the collector resistivity is calculated with the use of an expression which appropriately models the peripheral spreading currents. Various expressions are available [20], [21].



4.13. Collector Spreading Resistor (Large), Structure 3.18

Collector spreading resistor (large), structure 3.18, is a three-terminal resistor. Its design is similar to that of structure 3.12, section 4.12.



4.14. Collector Resistor (DGR), Structure 3.7

Collector resistor (DGR), structure 3.7, is a three-terminal resistor which consists of two emitters diffused into the collector. The collector resistivity and backside contact resistance are calculated from measurements which require perpendicular current flow beneath the center emitter and the backside. (This current is introduced at E_2.) Perpendicular current flow is established by adjusting the current through the peripheral emitter E_3, a diffused guard ring (DGR), and the backside so that the voltage difference between E_3 and E_2 is zero. If the backside contact resistance is negligible, the collector resistivity, ρ, is calculated from

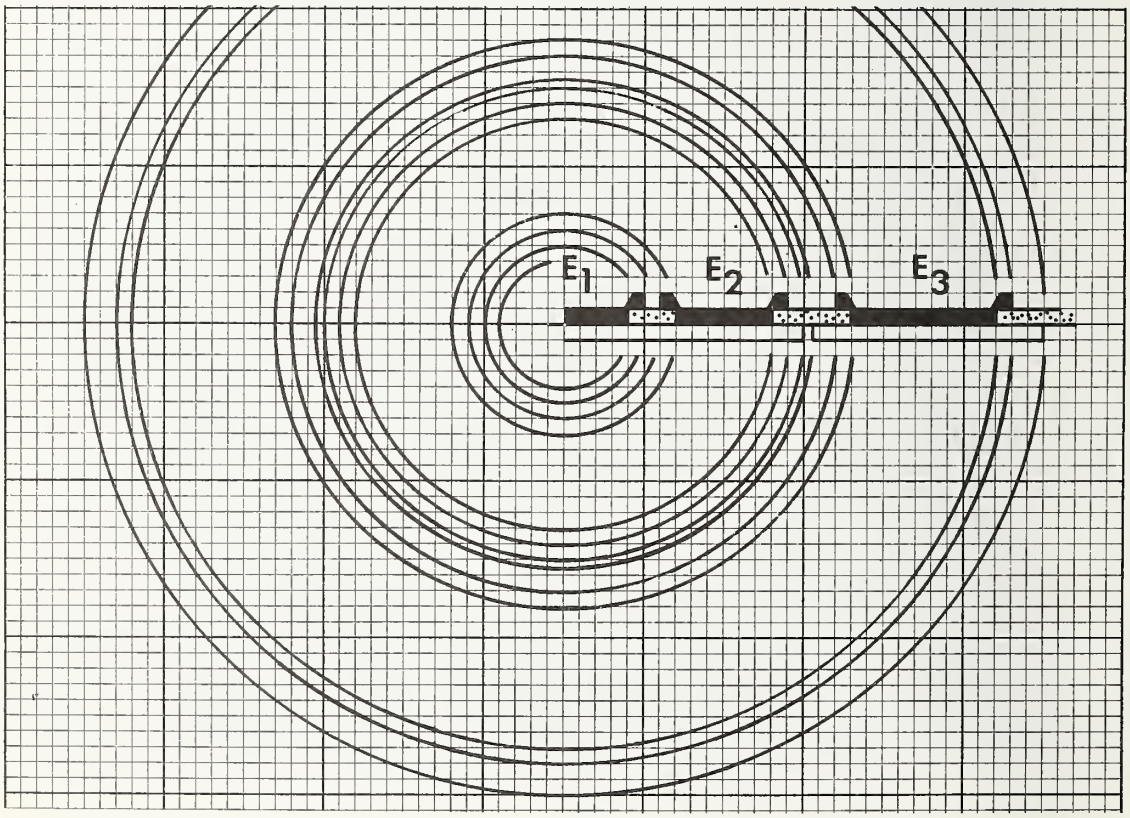
$$\rho = (V/I)(A/X_t) \tag{9}$$

where V is the voltage difference between E_1 and the backside, I is the curren into E_2, X_t is the thickness of the silicon between the emitter and the backside of the wafer, and A is the effective area of the center emitter. From the theory of the guarded capacitor [23] a good estimate for A is obtained by using the geometrical mean of the inner and outer radii of the gap between the center emitter and peripheral emitter. If the collector resistivity, ρ, is known from an independent measurement (e.g., structure 3.17), then the backside contact resistance, R_c, is calculated from

$$R_c = R_m - \rho X_t/A \tag{10}$$

where R_m is the measured resistance given by V/I as explained above.

In this measurement the center emitter must be an equipotential surface. This is achieved by heavily doping the emitter and by using thick metal. The placement of probes and the use of multiple probes to contact the same metal areas are important in achieving an equipotential surface.



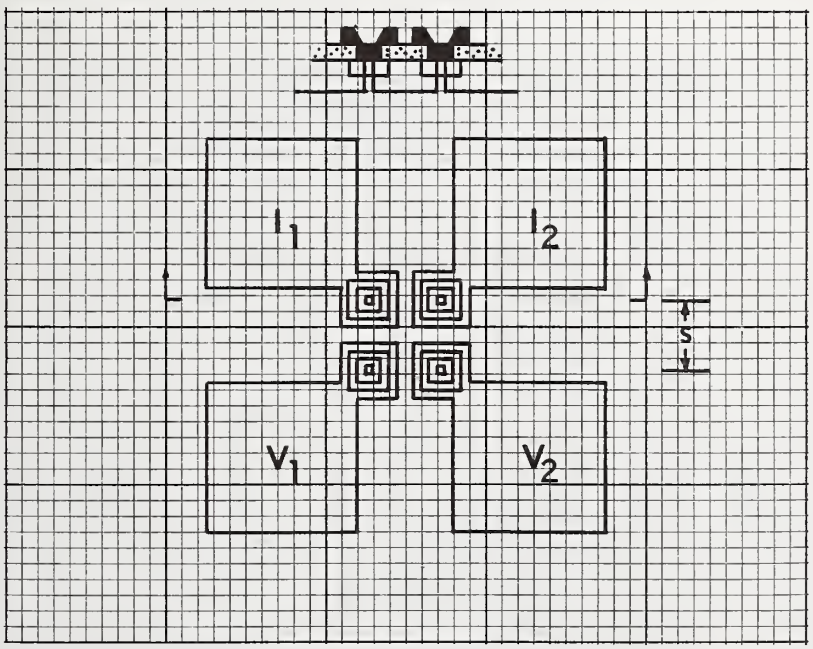
4.15. Collector Four-Probe Resistor, Structure 3.17

Collector four-probe resistor, structure 3.17, is a four-terminal resistor with four point contacts arranged in a square array. It is intended for the evaluation of the collector resistivity. This structure is fabricated by diffusing a base over a large area except at the four point contacts which are protected from the base diffusion by four base-oxide islands. Emitters are diffused at these points in order to make low resistance contact to the collector material. The purpose of the base diffusion is to eliminate surface currents. The collector resistivity, ρ, is calculated from [24]

$$\rho = (V/I)(2\pi s)/(2-\sqrt{2}) \qquad (11)$$

where the potential, V, is V_1-V_2 for a current, I, passed into I_1 and out of I_2 and s is the probe spacing. The spacing is taken as the center-to-center distance of 2.25 mil (57.2 μm). The above formula assumes that the thickness of the silicon wafer is large compared to the probe spacing and that the shorting effect of the backside metallization is negligible. For a wafer thickness, X_t, greater than or equal to 9.0 mil (229 μm), where $X_t/s \geq 4$, the correct resistivity when the backside is metallized is less than 0.6 percent larger than the measured resistivity. When the backside is not metallized the correct resistivity for $X_t/s \geq 4$ is less than 0.8 percent smaller than the measured resistivity [25]. The collector resistivity value calculated from the above formula does not depend on the backside contact resistance which does affect structures 3.1, 3.7, 3.12, and 3.18. The proper fabrication of structure 3.17 depends on the fabrication of a bipolar transistor with finite gain. This insures that the emitter has not been punched through the base and consequently that the current passes into the collector through a narrow channel.

A BASE (modified) mask was designed with oversize base-oxide islands which are squares 0.50 mil (12.7 μm) on a side. The details of this mask were discussed in the Introduction. As shown below the base-oxide islands are squares 0.25 mil (6.4 μm) on a side.



4.16. Collector Hall Effect Resistor, Structure 3.26

Collector Hall effect resistor, structure 3.26, is a four-terminal resistor formed when this test pattern, fabricated on a silicon wafer, is scribed into a square chip 100 mil (2.54 mm) on a side. The backside metal must be removed for this structure to operate properly. Scribe lines were purposefully omitted from the BASE and EMITTER masks to prevent doping the periphery of this structure. Contacts are formed in the four corners by an emitter diffused in a square 4.5 mil (114 μm) on a side. (This is the net size of the emitter contacts after the wafer is scribed into chips where the chip has separated in the middle of the scribe line.) For this case the ratio of the length of the contact to the length of the chip is 0.045. For this ratio the correction factor for the Hall coefficient is less than 2 percent and the correction factor for the resistivity is much less than 1 percent [26]. The resistivity, ρ, is calculated from [12]

$$\rho = (V_\rho/I)(\pi X_t/\ell n 2) \tag{12}$$

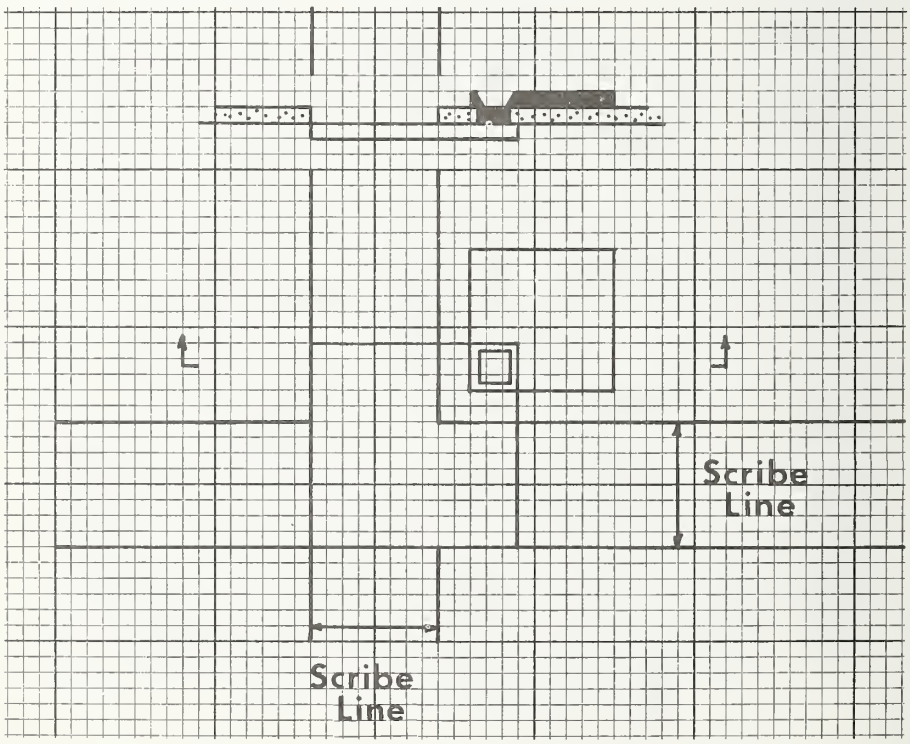
where X_t is the wafer thickness, V_ρ is the voltage difference measured between nearest neighbor contacts for a current, I, passed between the remaining two contacts. The Hall coefficient, R_H, is calculated from [12]

$$R_H = (V_H X_t)/(BI) \tag{13}$$

where V_H is the voltage difference measured between opposite contacts for a current, I, passed between the remaining two contacts and B is the magnetic field density perpendicular to the plane of the chip. The collector dopant density, N, is calculated from

$$N = r/[q|R_H|] \tag{14}$$

where q is the electronic charge and r is the scattering factor [8], [9]. The recommended measurement procedures for these measurements are described elsewhere [13].



5. MOS CAPACITORS

5.1. MOS Capacitor Over Collector (FP, CS), Structure 3.8

MOS capacitor over collector (FP, CS), structure 3.8, consists of a main gate, G_1, 15.0 mil (381 μm) in diameter which is surrounded by a field plate (FP), G_2 that overlaps a channel stop (CS) which also serves as a topside collector, C, contact. The collector dopant density, N, is calculated from the high frequency C-V C_{max}-C_{min} method [7] by using the transcendental relation:

$$\frac{C_o}{C_i} = 1 + \frac{C_o}{A}\left[\frac{4kT}{\varepsilon_s q^2 N}\ln\left(\frac{N}{n_i}\right)\right]^{1/2} \tag{15}$$

where C_o is the maximum (oxide) capacitance, C_i is the minimum (inversion) capacitance, A is the main gate area, k is the Boltzmann constant, T is temperature, ε_s is the silicon dielectric constant, q is the electronic charge, and n_i is the intrinsic carrier concentration. The value for N calculated from this method is a surface value which may be different from the bulk value due to dopant redistribution during oxidation [7].

To determine the bulk collector value a dopant profile is obtained by use of the high frequency C-V deep depletion method [6] where the collector dopant density, $N_i(W)$, in an incremental region is calculated from

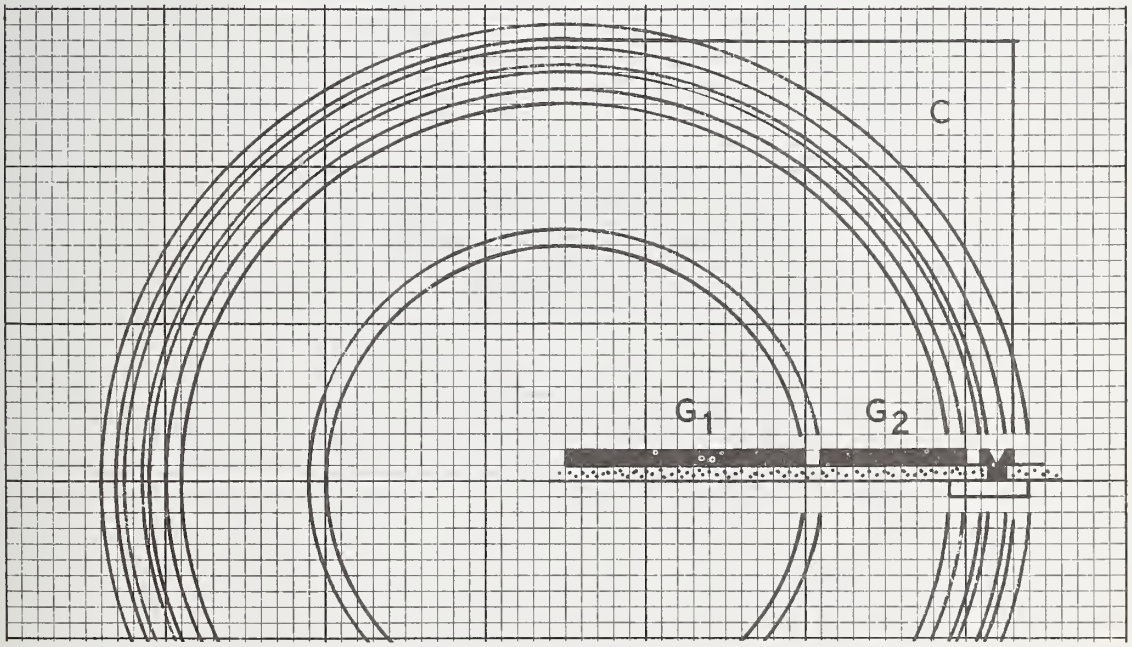
$$N_i(W) = (2/q\varepsilon_s A^2)[\Delta V/\Delta(C^{-2})] \tag{16}$$

where ΔV is an incremental change in the gate voltage. The measured MOS capacitance, C, is

$$C^{-1} = C_o^{-1} + C_s^{-1} \tag{17}$$

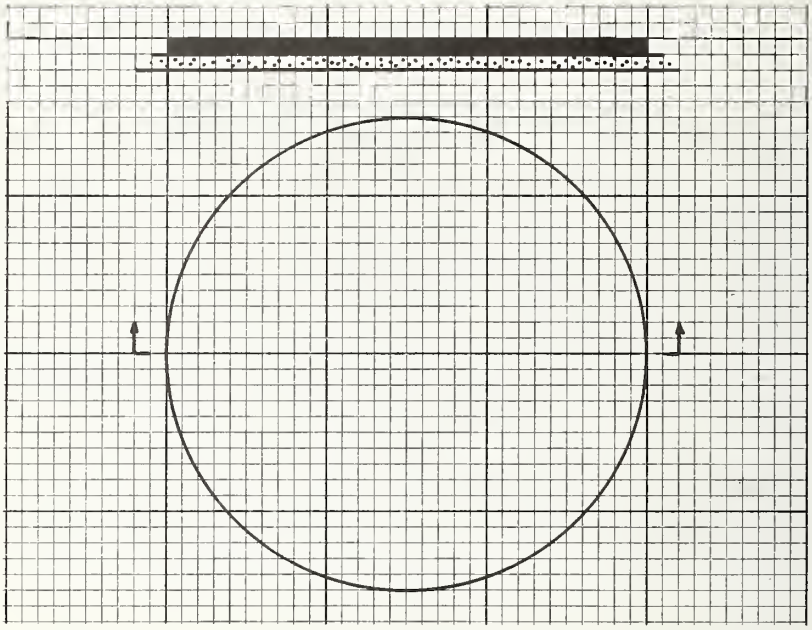
where C_s is the semiconductor capacitance. The depth, W, from the oxide-silicon interface to the edge of the depletion region is

$$W = \varepsilon_s A/C_s. \tag{18}$$



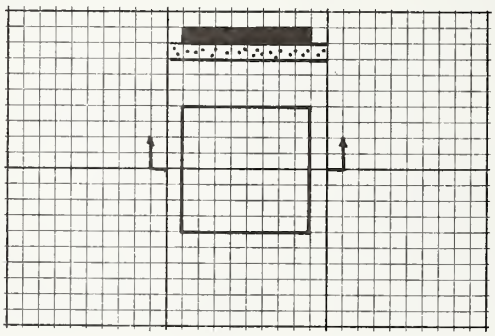
5.2. MOS Capacitor Over Collector, Structure 3.19

MOS capacitor over collector, structure 3.19, consists of a circular main gate 15.0 mil (381 μm) in diameter without a peripheral field plate. This structure is useful in evaluating charge spreading (ion migration) phenomena [27].



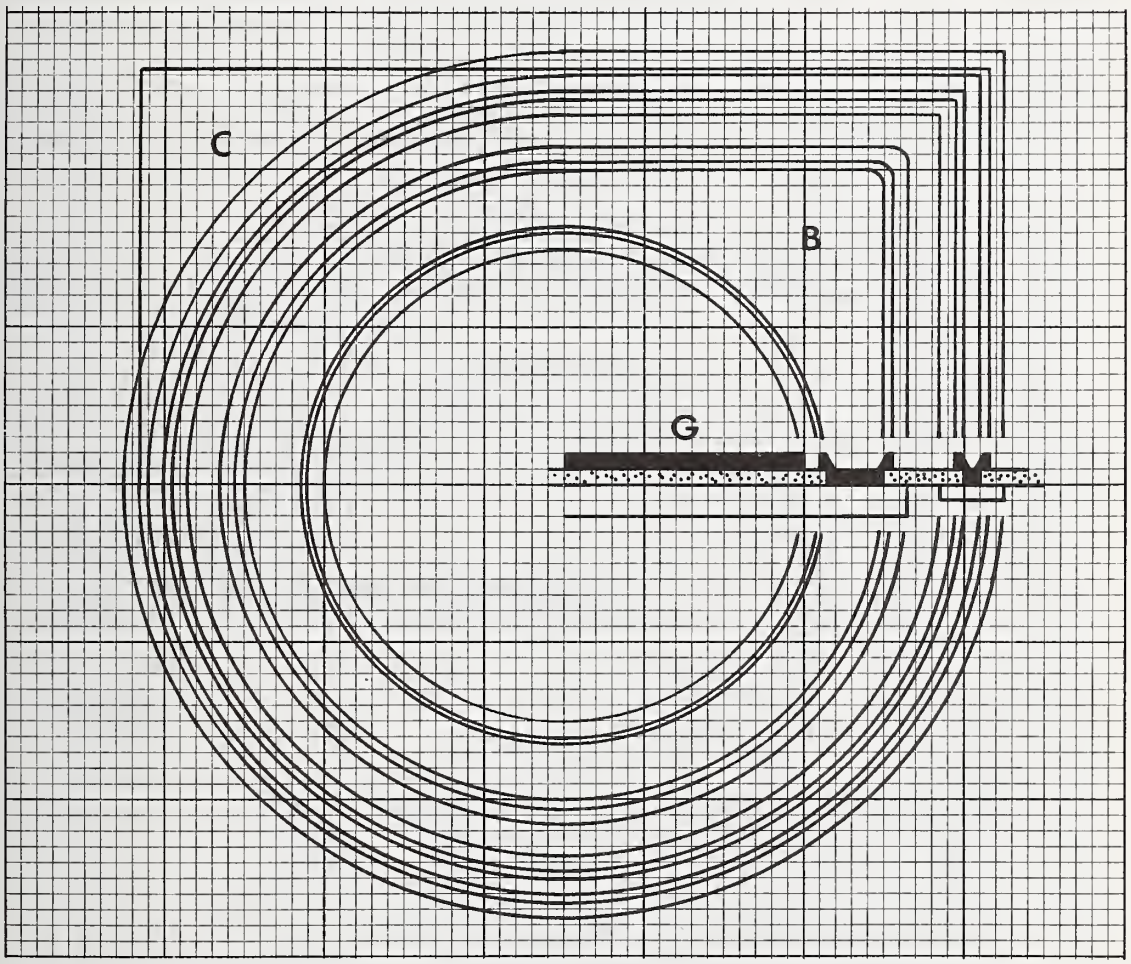
5.3. MOS Capacitor Over Collector, Structure 3.25

MOS capacitor over collector, structure 3.25, consists of a small square main gate 4.0 mil (102 μm) on a side without a peripheral field plate. This structure is useful in evaluating measurement limitations due to small gate areas.



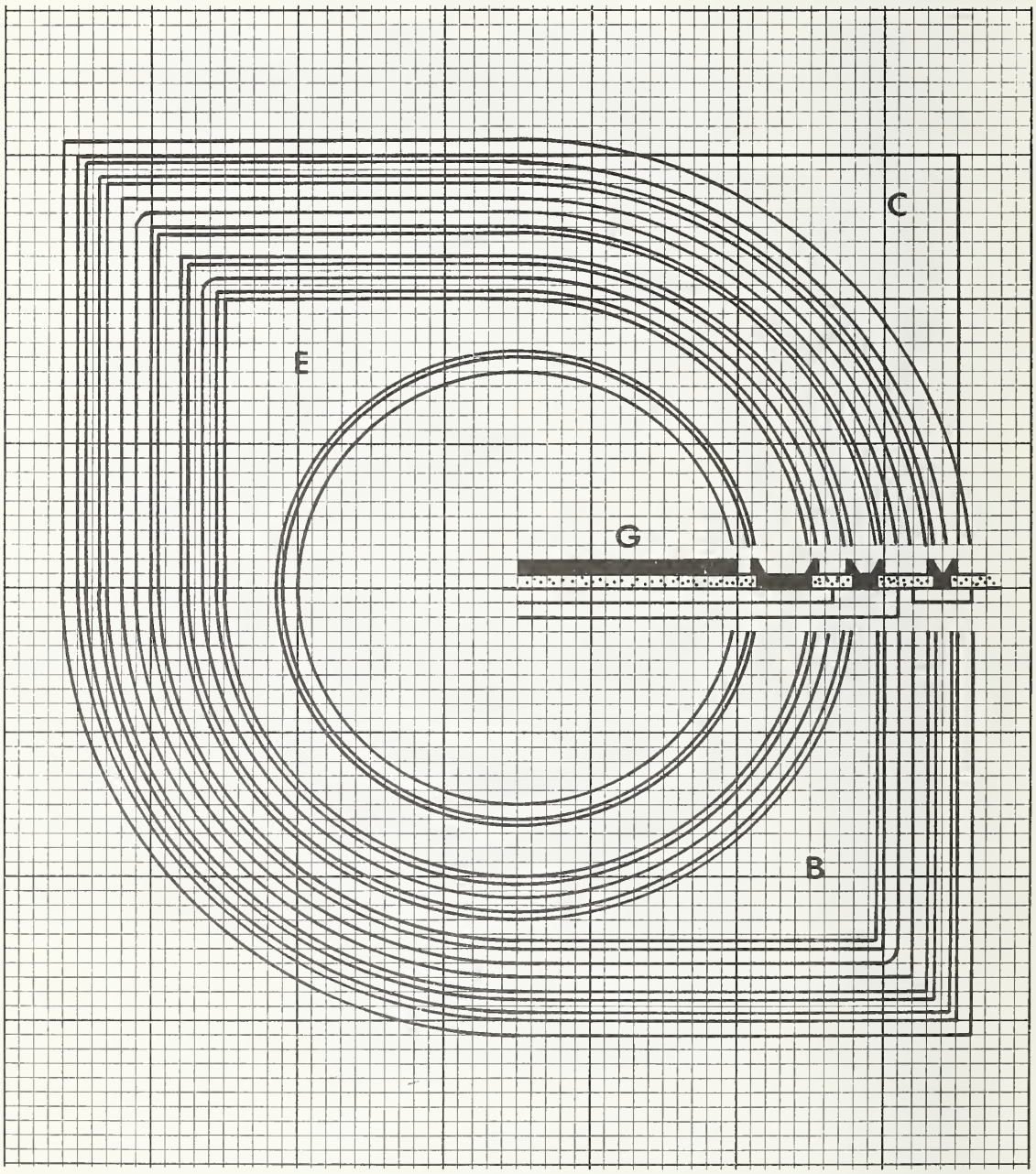
5.4. MOS Capacitor Over Base, Structure 3.2

MOS capacitor over base, structure 3.2, consists of a metal gate, G, 15.0 mil (381 μm) in diameter on top of an oxide layer over a diffused base, B. A diffused emitter surrounds the base and serves as a topside collector, C, contact. This structure is used to evaluate the base surface dopant density by the methods described in section 5.1 for structure 3.8. This structure is also useful as a base-oxide pinhole test. It can also be used for base-collector diode C-V measurements; however, the junction area calculation is somewhat complicated by the fact that the junction is not circular.



5.5. MOS Capacitor Over Emitter, Structure 3.3

MOS capacitor over emitter, structure 3.3, consists of a metal gate, G, 15.0 mil (381 μm) in diameter on top of an oxide grown over a diffused emitter, E. Topside contact is provided to both the emitter and base. A diffused emitter surrounds the base and serves as a topside collector, C, contact. This structure is used to evaluate the emitter surface dopant density by the methods described in section 5.1 for structure 3.8. This structure is also useful as an emitter oxide pinhole test and as a bipolar transistor.



6. DIODES

6.1. Base-Collector Diode (FP, CS), Structure 3.10

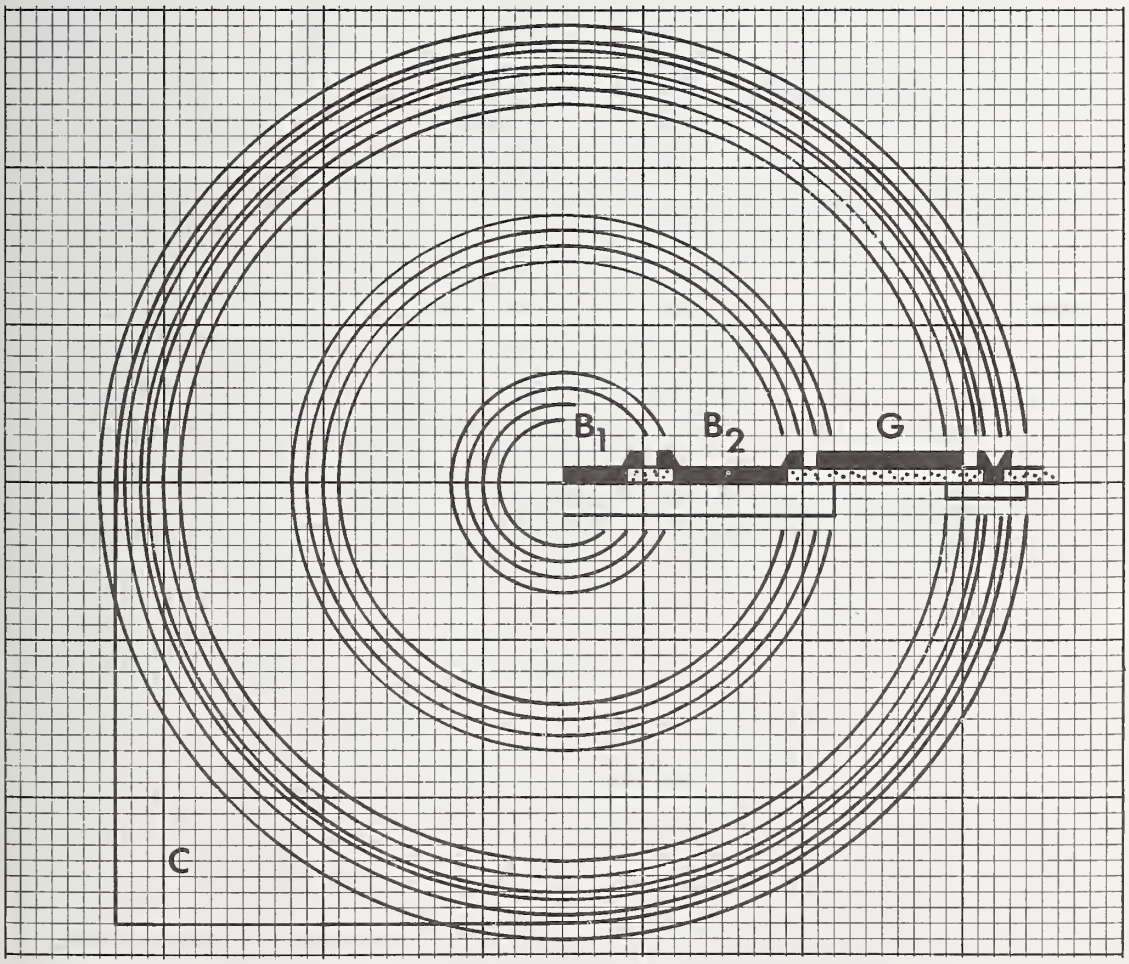
Base-collector diode (FP, CS), structure 3.10, consists of a base 17.0 mil (432 μm) in diameter diffused into a collector and a metal field plate (FP), G, to control the periphery. The field plate overlaps both the base and a diffused emitter channel stop (CS) which also serves as a topside collector, C, contact. The collector dopant density, $N_i(W)$, in an incremental region is calculated from the Schottky equation:

$$N_i(W) = (2/q\varepsilon_s A^2)[\Delta V/\Delta(C^{-2})] \qquad (19)$$

where ΔV is an incremental change in the applied voltage, C is the junction capacitance, q is the electronic charge, ε_s is the dielectric constant of silicon, and A is the area of the base. The effective depth, W, is taken, in the simplest case of a one-side junction, as

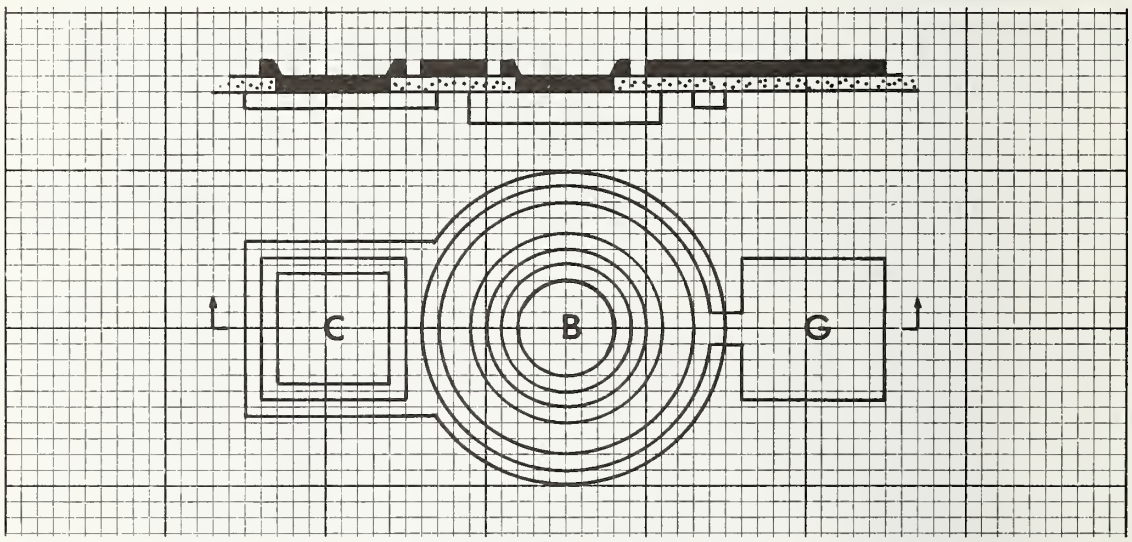
$$W = \varepsilon_s A/C. \qquad (20)$$

For junctions found in practice, peripheral capacitance and diffused layer effects may be taken into account by a model and computer program detailed elsewhere [28]. To obtain a correct profile the field plate must be biased at the flat-band potential [5].



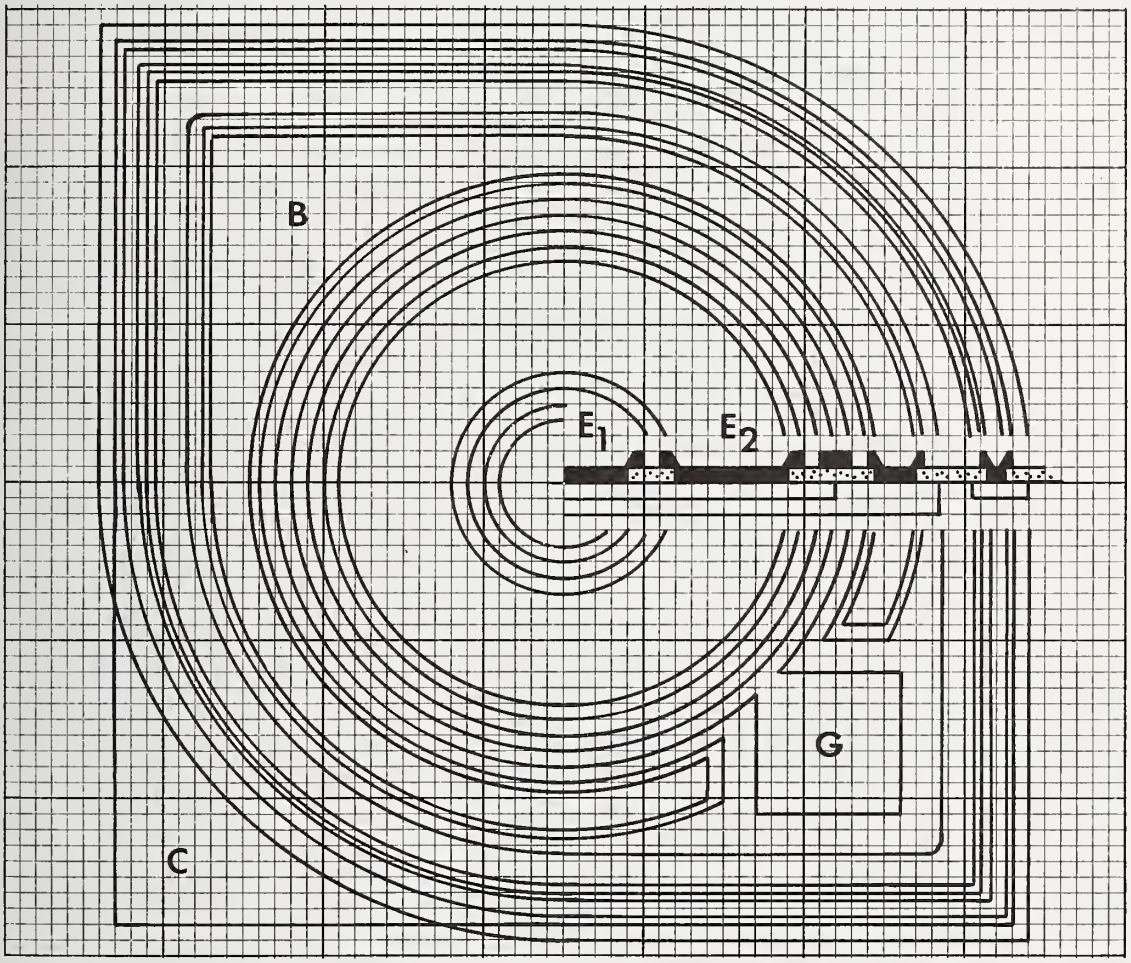
6.2. Base-Collector Diode (FP, CS), Structure 3.14

Base-collector diode (FP, CS), structure 3.14, consists of a base 5 mil (127 μm) in diameter diffused into a collector. This structure is a miniature version of structure 3.10 described in section 6.1 The metal field plate (FP), G, has a metallized contact which extends over the collector. The field plate controls the periphery of the junction and extends from the base to the diffused emitter channel stop (CS) which serves as a topside collector, C, contact. The base is large enough so that its metallization is confined within the base diffusion. This allows precise measurement of the junction capacitance needed in the computation of dopant density values.



6.3. Emitter-Base Diode (FP), Structure 3.9

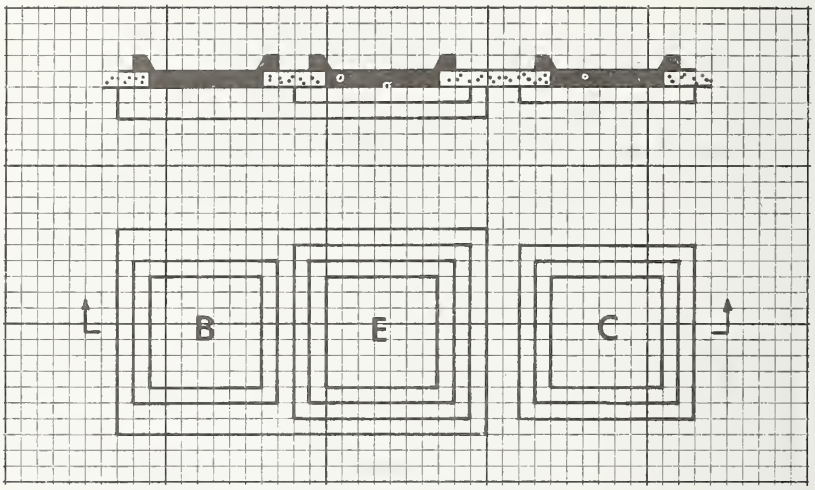
Emitter-base diode (FP), structure 3.9, consists of an emitter 17.0 mil (432 μm) in diameter diffused into a base and a field plate, G, to control the periphery of the emitter. This structure is intended to be used to obtain base dopant profiles by the method described in section 6.1 for structure 3.10. The use of this method for obtaining base dopant profiles should be approached with caution in the light of recently published work [29].



7. TRANSISTORS

7.1. Bipolar Transistor, Structure 3.13

Bipolar transistor, structure 3.13, consists of a square emitter, E, 5.5 mil (140 μm) on a side diffused into a base, B, and an emitter diffused into a collector to provide topside collector, C, contact. This vertical transistor is intended to verify that the emitter and base diffusions have formed a transistor structure with finite gain. This is one of the requirements needed to insure the proper fabrication of the collector four-probe resistor, structure 3.17, described in section 4.15.



7.2. Tetrode Transistor, Structure 3.6

Tetrode transistor, structure 3.6, consists of a donut shaped emitter [30] with an inside diameter of D_1 = 6.0 mil (152 μm) and an outside diameter of D_2 = 17.0 mil (432 μm) diffused into a circular base 23.5 mil (597 μm) in diameter. This structure is intended to be used to obtain the sheet resistance, R_S, of the base-under-emitter which can be calculated from

$$R_S = (V/I)[2\pi/\ell n(D_2/D_1)] \tag{21}$$

where V is the potential drop between the center, B_1, and outer, B_2, base contacts for a current, I, passed between these contacts. This structure is a two-terminal resistor, but interference due to the contact resistance is negligible because the contact resistance is usually much smaller than the sheet resistance.

The incremental resistivity can also be measured in a narrow region of the base by adjusting the width of the base region which is conducting current. This is accomplished by changing the bias across the emitter-base junction which varies the width of the emitter-base depletion region. The base resistivity, $\rho_i(W)$, in an incremental region is calculated from

$$\rho_i(W) = \frac{2\varepsilon_S \pi A}{\ell n(D_2/D_1)} \frac{\Delta(C^{-1})}{\Delta(R^{-1})} \tag{22}$$

where ε_S is the dielectric constant of silicon, R = V/I, A is the area of the emitter-base junction, and C is the capacitance of the emitter-base junction. This expression is similar to those derived by others [11]. The incremental region is located at a distance W from a one-sided junction.

This distance, W, is given by

$$W = \varepsilon_s A/C. \tag{23}$$

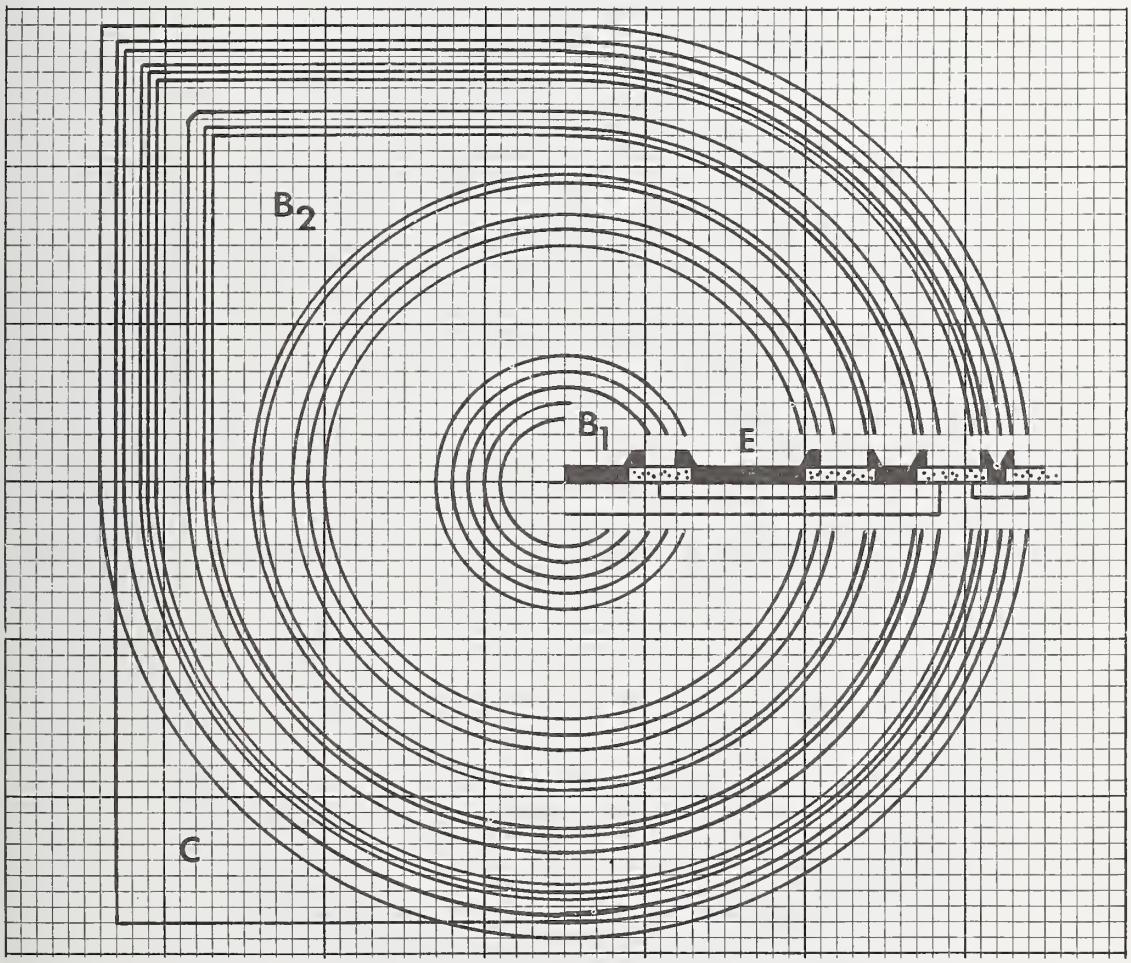
The base dopant density, $N_i(W)$, for the incremental region located at W is given by

$$N_i(W) = (2/q\varepsilon_s A^2)(\Delta V/\Delta C^{-2}) \tag{24}$$

where ΔV is the change in the voltage across the emitter-base junction. The above equations for $\rho_i(W)$ and $N_i(W)$ yield a variety of values for the resistivity versus dopant density relation. These relations for $\rho_i(W)$ and $N_i(W)$ may be combined to yield mobility profiles, $\mu_i(W)$, through the base as given by

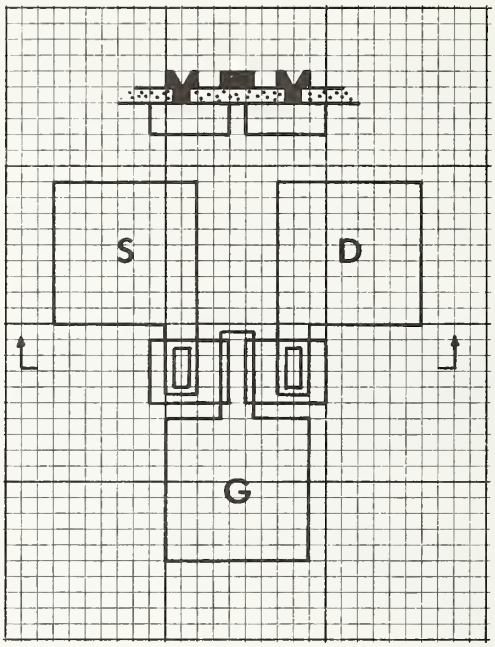
$$\mu_i(W) = 1/q\rho_i N_i \tag{25}$$

where q is the electronic charge. Due to increased crystalline dislocations and other impurity scattering centers in base regions, the mobilities measured here are expected to be lower than in bulk silicon.



7.3. MOS Transistor, Structure 3.16

MOS transistor, structure 3.16, consists of base diffusions which serve as a source, S, and drain, D. The gate, G, has a photomask W/L ratio of 4 where L = 0.50 mil (12.7 μm). This structure is intended to simulate the electrical characteristics of a typical integrated circuit device.

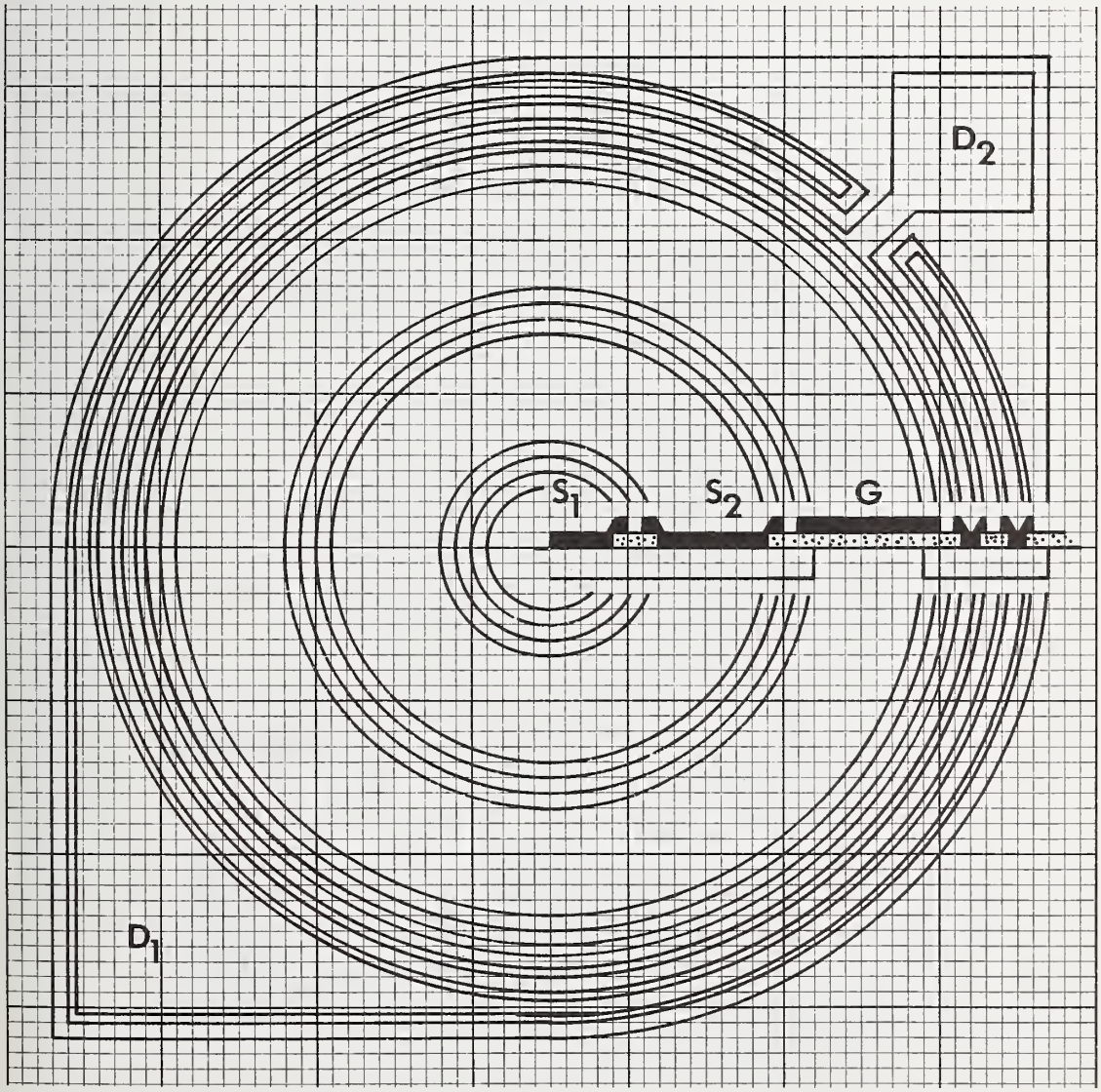


7.4. MOS Transistor, Structure 3.15

MOS transistor (circular), structure 3.15, consists of base diffusions which serve as source, S_1 and S_2, and drain, D_1 and D_2, and a gate, G. This structure, being circular, has an edgeless gate region which simplifies the geometrical calculation associated with the current flow. The effective photomask W/L ratio is $2\pi/ln(R_2/R_1)$ where the inside radius of the drain, R_2, is 12 mil (305 μm) and the radius of the source, R_1, is 8.5 mil (216 μm), so that W/L = 18.22. The source and drain regions have dual metal contacts that allow four-terminal measurements of the inversion region channel mobility. From the measurement of the low voltage transconductance, $G_o = I_{DS}/V_{DS}$, as a function of gate voltage, V_{GS}, the channel mobility, μ, can be calculated from [31]

$$\mu = (X_{oc}L/\varepsilon_o W)(\Delta G_o/\Delta V_{GS}) \qquad (26)$$

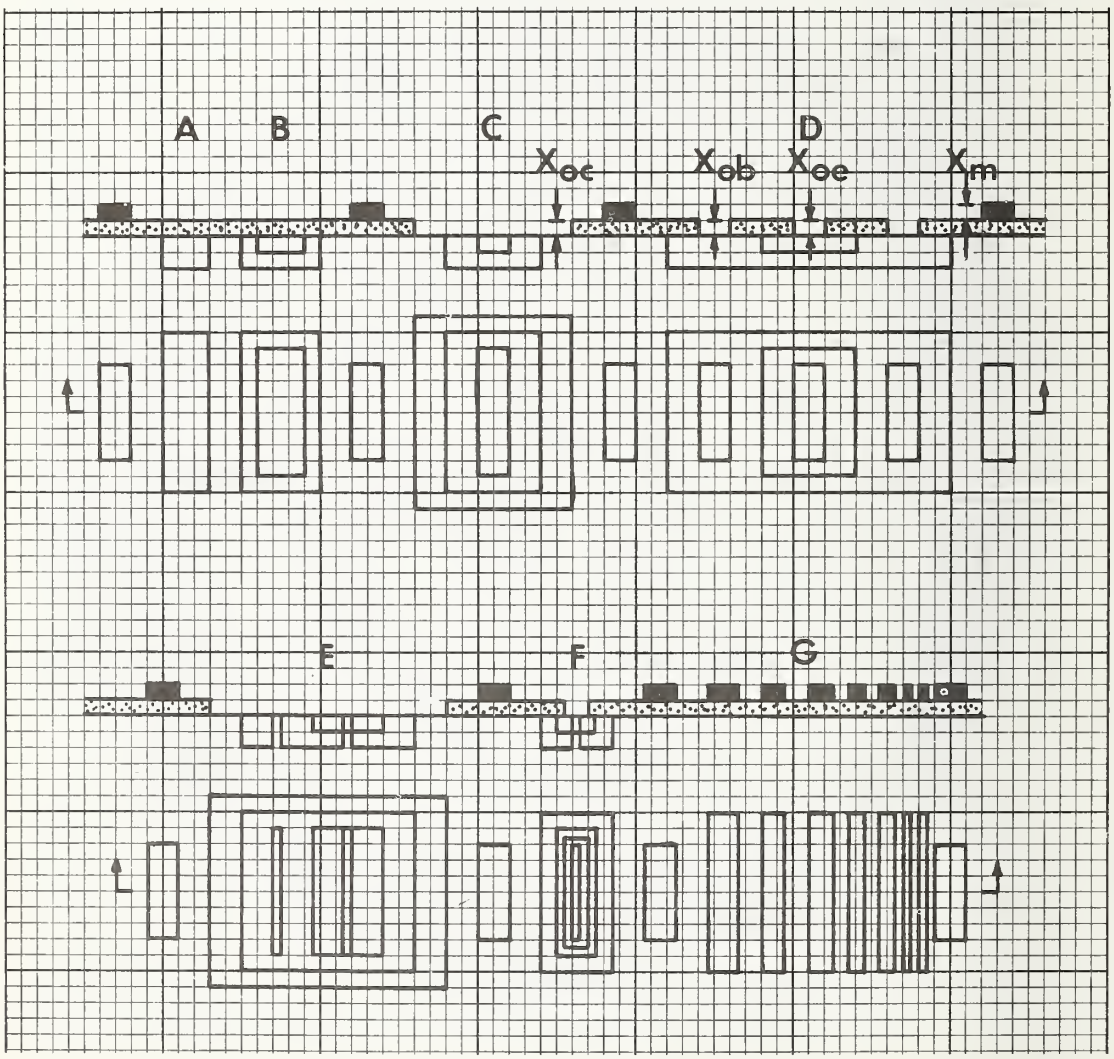
where ΔV_{GS} is the incremental change in the gate to source voltage, X_{oc} is the collector oxide thickness and ε_o is the oxide dielectric constant. The gate oxide thickness may be determined from structure 3.29, section 8.1, or from structure 3.8, section 5.1, using $X_{oc} = \varepsilon_o A/C_o$.



8. MISCELLANEOUS

8.1. Surface Profilometer Structure, Structure 3.29

Surface profilometer structure, structure 3.29, consists of a region where a mechanical stylus-type profilometer is used to evaluate various regions for process control and diagnostic purposes. The cross sectional drawing of this structure as shown below is a schematic view, for the silicon surface is shown flat. In fact the silicon surface does vary due to the incorporation of silicon into the oxide during various oxidation steps. (This is illustrated by the profile shown on page 38.) The surface contour over the base oxide is obtained from (A) and over the emitter oxide is obtained from (B). The surface contour of the silicon surface over collector, base, and emitter are obtained from (C). The thickness of various layers is determined from (D): X_{oe} is the oxide thickness over the emitter, X_{ob} is the oxide thickness over the base, X_{oc} is the oxide thickness over the collector, and X_m is the metal thickness. For diagnosing the smallest geometry structure, 3.17, the critical portion of this structure is elongated in one direction as seen in (E) and (F). In (E) the oxide is removed and in (F) the metal is removed. A metal resolution pattern is seen in (G). Between each structure a metal marker is provided for easy identification of structures.



8.2. Etch-Control Structures 3.31 B, E, C, M

Etch-control structures, structures 3.31 B, E, C, M, consist of squares offset by multiples of 0, 1, and 2 times 0.25 mil (6.4 μm). The layout of the BASE, EMITTER, and CONTACT oxide etch structures is identical; for these structures over-etch causes the squares to increase in size. This effect is illustrated in figure 5.

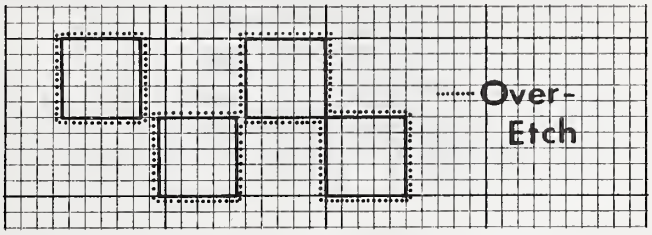
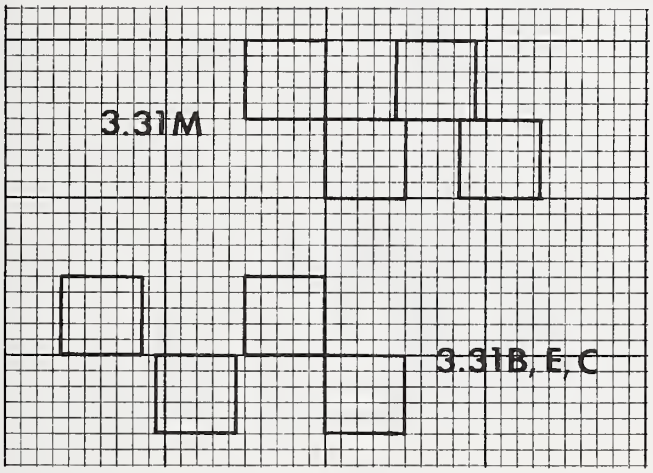


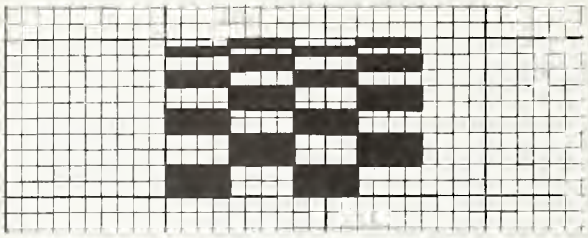
Figure 5. Etch-control structure where the regions within the squares were etched out so as to increase the size of the squares to the dotted lines.

The layout of the METAL etch structure is different, for over-etch causes these squares to decrease in size. The alignment of the sides of adjacent squares indicates that the over-etch is between 0 and 0.125 mil (3.2 μm) or between 0.125 mil (3.2 μm) and 0.25 mil (6.4 μm) or greater than 0.25 mil (6.4 μm). As illustrated in figure 5, the amount of over-etch is 0.125 mil (3.2 μm). These patterns provide a rapid visual indication of over-etch problems, since the amount of over-etch is easily determined.



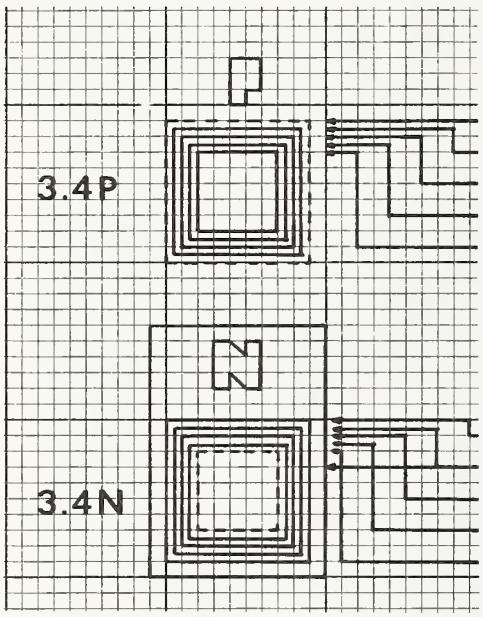
8.3. Resolution Structures, Structure 3.32 B, C, M

Resolution structures, structures 3.32 B, C, M, consist of offset rectangles which are spaced in multiples of 1, 2, 3, and 4 times 0.25 mil (6.4 μm). This pattern is found on the BASE, CONTACT, and METAL masks and indicates the quality of the photolithographic and etching processes.



8.4. Alignment Markers, Structures 3.4 N, P

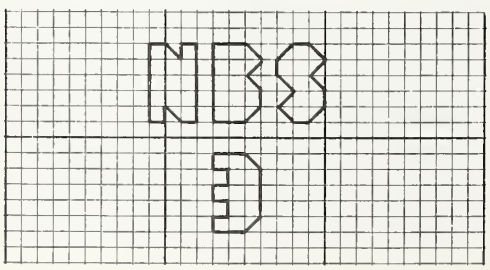
Alignment markers, structures 3.4 N, P, consist of concentric squares whose sides differ by 0.5 mil (13 μm). Two markers are present; one for use with positive photoresist, indicated by a P, and another for use with negative photoresist, indicated by an N.



MASK	WITHIN SQUARE
PASSIVATION	(CLEAR)
CONTACT	(CLEAR)
EMITTER	(CLEAR)
BASE	(CLEAR)
METAL	(BLACK)
METAL	(CLEAR)
BASE	(BLACK)
EMITTER	(BLACK)
CONTACT	(BLACK)
PASSIVATION	(BLACK)

8.5. NBS Logo, Structure 3.5

NBS logo, structure 3.5, consists of the symbols NBS formed in the metalization.



9. AN *n-p-n* TRANSISTOR FABRICATION PROCESS

Recall that the main objective of this test pattern is to evaluate the resistivity-dopant density relation in *n*- and *p*-type bulk silicon over the dopant density range from less than 10^{14} to above 10^{20} cm^{-3}. To accomplish this task an *n-p-n* transistor process and a *p-n-p* transistor process were developed. To illustrate the use of this pattern the *n-p-n* transistor process is described.

The fabrication process is outlined in table 2 which indicates the steps in the fabrication of an *n-p-n* transistor in a bulk, (111) oriented, nominally 10 Ω·cm, *n*-type silicon wafer. Target values are shown for the sheet resistance, R_S(Ω/□), the junction depth, X_j(μm), and the layer thickness, X(nm). In the fabrication process four photomasks were used: BASE (modified), EMITTER, CONTACT, and METAL. The wafer is also metallized on the backside to reduce the backside contact resistance. The cleanup steps involve an ammonium hydroxide-peroxide mixture followed by a hydrochloric acid-peroxide mixture [32]. The flow rate for steps 2, 5, 6, 9, 14 and 26 is 500 cm^3/min. The flow rates for step 12 are 3265 cm^3/min of N_2, 35 cm^3/min of O_2, and 200 cm^3/min of PH_3.

Table 2 - An *n-p-n* Transistor Wafer Fabrication Process

	Process Step	T, °C	Ambient	t, min	R_S, X_j, X, Ω/□, μm, nm
1.	Cleanup (ultrasonic)				
2.	Oxidation (25 ml H_2O)	1100	O_2(W), O_2, N_2	20, 20, 20	-, -, 350
3.	BASE photoresist			2.5	
4.	Cleanup				
5.	BN preparation (A-type)	965	N_2	30	
6.	Boron deposition	965	N_2	25	50, -, -
7.	Deglaze (10% HF)			0.5	
8.	Rinse (DI; spin dry under N_2)			5	
9.	Drive-in diffusion (25 ml H_2O)	1100	O_2(W), O_2, N_2	20, 40, 20	200, 2, 360
10.	EMITTER photoresist			3	
11.	Cleanup				
12.	Phosphorus diffusion (PH_3)	1000	N_2 O_2 PH_3	20	
13.	Deglaze (10% HF)			0.2	
14.	Oxidation (steam)	925	O_2(W), O_2, N_2	30, 5, 10	10, 1, 220
15.	CONTACT photoresist			3	
16.	Cleanup				
17.	Topside Al evaporation (E-gun)				-, -, 800
18.	METAL photoresist				
19.	Wax wafer face down				
20.	Backside oxide removal (1:1 DI:HF)			0.75	
21.	Rinse (DI; spin dry under N_2)				
22.	Backside silicon removal (CP-6)				
23.	Rinse (DI; spin dry under N_2)				
24.	Backside Au evaporation (filament) 0.6% Sb doped Au				-, -, 200
25.	Dewax (TCE, acetone cobaltous nitrate, DI)				
26.	Microalloy	500	N_2	30	

W = wet. CP-6 = 5:4.5:3 parts of HNO_3:Acetone Acid:HF. TCE = trichloroethylene. DI = deionized water.

10. TEST PATTERN NBS-3 MEASURED VALUES

In this section, test results obtained from various test structures are presented for the *n-p-n* transistor fabrication process described in the previous section. These measured values are intended to indicate the kind of information obtainable from this test pattern. More detailed measurements on some of the structures are presented elsewhere [5].

All electrical measurements were made in the dark at room temperature. The measured values, listed in table 3, represent the mean and one sample standard deviation of five measurements taken on a two-inch (5 cm) diameter silicon wafer. The measurements were taken at sites located at the top, bottom, left, middle, and right positions on the wafer where the distance between sites was 600 mil (15 mm). The measured values were calculated by using the formulas presented in sections 4 through 8.

The resistor test structures were measured by forcing a current in opposite directions through the structure and averaging the resulting voltages. For the van der Pauw and four-probe resistor structures, additional voltages were measured by shifting the voltage and current points to the next adjacent point. These voltages were then averaged with the first voltages.

As seen in table 3 the base sheet resistance values measured by use of the van der Pauw structures 3.11, 3.28, and 3.30 are close to 190 Ω/□. This verifies that the van der Pauw sheet resistance values are not dependent on the geometry of the structure. The base sheet resistance value measured by use of the bridge structure 3.28 is 173 Ω/□ which is lower than the van der Pauw values because a W_e of 1.50 mil (38.1 μm) was used in the bridge sheet resistance calculation. As calculated from equation (4), the effective width, W_e, of the base bridge structure is 1.64 mil (41.7 μm) due to the over-etch of the oxide window and lateral base diffusion. Similar remarks hold for the emitter sheet resistance where the van der Pauw value of 10.7 Ω/□ is higher than the bridge value of 9.8 Ω/□. The effective width, W_e, of the emitter bridge structure is 1.57 mil (39.9 μm). The emitter-oxide window was over-etched by W_{oe} = 0.06 mil (1.5 μm). The combination of measurements from the bridge and van der Pauw sheet resistance structures provides a rapid means for determining the width of oxide windows. Measurements on the orthogonal van der Pauw structures 3.20, 3.21, and 3.22 demonstrate that this structure is capable of evaluating sheet resistances which vary from 0.03 Ω/□ for the metallization to 190 Ω/□ for the base. The metal-to-base contact resistance of 1.5 μΩ·cm^2 is larger than the metal-to-emitter contact resistance of 0.18 μΩ·cm^2. The contact resistance values are intended as a qualitative check on the process, for they are influenced by many factors including the contact window area and the sheet resistance of the diffused layer. The step coverage resistance is an average of the resistances measured on the two resistors. Four-probe resistor measurements indicate that the *n*-type collector substrate resistivity is 11.2 Ω·cm; a probe spacing of 2.25 mil (57.2 μm) was used in the calculation. To validate these results the gain of the bipolar transistor, structure 3.13, was measured. A gain of 80 indicates that the emitter is not shorted to the collector.

Capacitance-voltage measurements were made on a variety of structures and various dopant densities were determined. The capacitances were measured at 1 MHz with the use of a 15 mV rms signal. The MOS capacitor over the collector (3.8) was measured by two methods. The dopant density, 4.7×10^{14} cm^{-3} determined from the C_{max}-C_{min} method is higher than the 4.3×10^{14} cm^{-3} value calculated from the deep-depletion method. The difference in these values is due to the region sampled by the two methods. The C_{max}-C_{min} method samples the dopant density near the oxide-silicon interface where phosphorus is piled up during the oxidation steps; the deep-depletion method samples the true collector substrate dopant density. Other MOS capacitor values are listed. The dopant density value determined from the small MOS capacitor, consisting of a square 4 mil (102 μm) on a side, is larger than values measured on the larger capacitors because the area and peripheral capacitance corrections

Table 3 - Measurements on Test Pattern NBS-3*

Test Structure	Equation	Conditions	Quantity Measured	Measured Value	Units
DP R, 3.22	(1)	I = 0.3 mA	Base R_s	189 ± 4	Ω/□
DP R, 3.11	(5)	I = 0.3 mA	Base R_s	189 ± 5	Ω/□
DP R, 3.30	(6)	I = 0.3 mA	Base R_s	190 ± 5	Ω/□
ridge R, 3.28	(2)	I = 0.2 mA, L/W_e = 4	Base R_s	173 ± 4	Ω/□
DP R, 3.21	(1)	I = 10 mA	Emitter R_s	10.7 ± 0.5	Ω/□
ridge R, 3.27	(2)	I = 0.5 mA, L/W_e = 4	Emitter R_s	9.8 ± 0.5	Ω/□
DP R, 3.20	(1)	I = 100 mA	Metal R_s	0.0336 ± 0.0006	Ω/□
etrode T, 3.6	(21)	I = 0.04 mA	Base-under-emitter R_s	3400 ± 160	Ω/□
.22, 3.28	(4)	L(mask) = 6 mil	Base W_e	1.64 ± 0.01	mil
.22, 3.28	(3)	α = 0.3	Base W_{oe}	0.12 ± 0.01	mil
.21, 3.27	(4)	L(mask) = 6 mil	Emitter W_e	1.57 ± 0.01	mil
.21, 3.27	(3)	α = 0.3	Emitter W_{oe}	0.06 ± 0.01	mil
ontact R, 3.24	(8)	I = 50 mA, A = 1 mil^2	Metal-to-base R_c	1.45 ± 0.05	μΩ·cm^2
ontact R, 3.23	(8)	I = 50 mA, A = 1 mil^2	Metal-to-emitter R_c	0.177 ± 0.005	μΩ·cm^2
etal R, 3.33	-	I = 8 mA	Metal step coverage R	1.61 ± 0.02	Ω
-Probe R, 3.17	(11)	I = 0.070 mA	Collector ρ	11.2 ± 0.5	Ω·cm
ransistor, 3.13	-		Common emitter gain	80 ± 10	-
OS C, 3.8	(15)	C_{max}-C_{min}	Collector N	4.69 ± 0.29 × 10^{14}	cm^{-3}
OS C, 3.8	(16)	Deep depletion	Collector N	4.35 ± 0.18 × 10^{14}	cm^{-3}
OS C, 3.19	(16)	Deep depletion	Collector N	4.43 ± 0.17 × 10^{14}	cm^{-3}
OS C, 3.25	(15)	C_{max}-C_{min}	Collector N	5.62 ± 0.38 × 10^{14}	cm^{-3}
OS C, 3.2	(16)	Deep depletion	Base N	2.41 ± 0.4 × 10^{18}	cm^{-3}
iode, 3.10	(19)		Collector N	4.36 ± 0.25 × 10^{14}	cm^{-3}
iode, 3.14	(19)		Collector N	1.26 ± 0.72 × 10^{15}	cm^{-3}
rofile, 3.29			Emitter oxide X_{oe}	260 ± 10	nm
rofile, 3.29			Base oxide X_{ob}	360 ± 10	nm
rofile, 3.29			Collector oxide X_{oc}	420 ± 10	nm
rofile, 3.29			Metal X_m	770 ± 10	nm
-			Emitter X_{je}	1.23 ± 0.05	μm
-			Base X_{jb}	2.00 ± 0.05	μm
-			Base width X_{jbe}	0.90 ± 0.05	μm
-			Wafer X_t	10.6 ± 0.1	mil

Wafer 44. L(mask) = 6.0 mil (152 μm). A = 1 mil^2 = 6.5 × 10^{-6} cm^2. The symbol N refers to the dopant density not the conductivity type.

were not taken into account. The base surface dopant density, 2.4×10^{18} cm^{-3} was determined from the MOS capacitor over the base. Dopant density values were calculated from capacitance-voltage measurements taken on diodes 3.10 and 3.14. Equation (19) was used to evaluate the C-V data which were not corrected for peripheral capacitance or diffused layer effects. These effects have a minimal effect on the dopant density value derived from the large diode 3.10; this dopant density agrees with values obtained from the MOS capacitors. The dopant density value derived from the small diode 3.14 is too high because the peripheral capacitance correction was not taken into account [5].

The thickness of various layers was obtained from the surface profilometer structure 3.29 by use of a mechanical stylus-type profilometer. The thickness of the metallization, X_m, the oxide thickness over the emitter, X_{oe}, the oxide thickness over the base, X_{ob}, and the oxide thickness over the collector, X_{oc}, are listed in table 3. A profile of structure 3.29 is shown in figure 6 along with a schematic cross section. The profile shows in D the thickness of various layers, in C the contour of the silicon surface, in E and F the base-oxide islands, and in G the resolution of the metal pattern. The BASE (modified) mask was used where the base-oxide islands are squares 0.50 mil (12.7 μm) on a side. The smallest line width on the metal pattern is 0.25 mil (6.4 μm), and this line was clearly resolved. The roughness of the aluminum metallization is indicated by the spikes protruding from the metal.

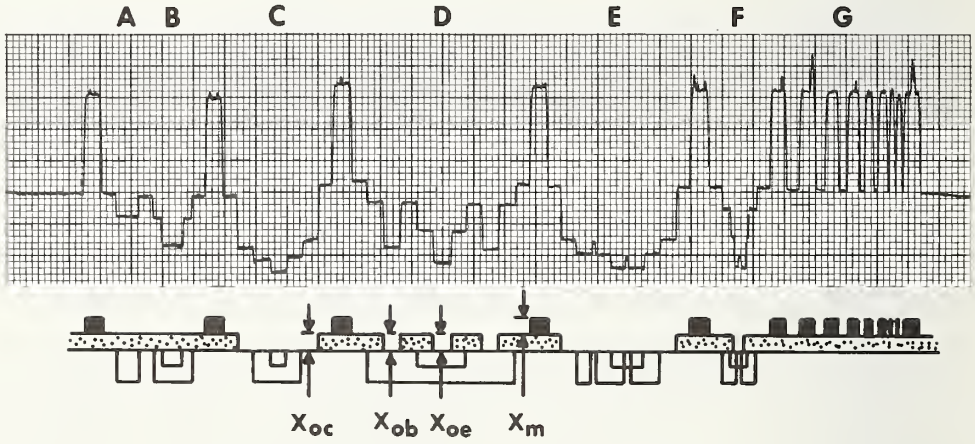


Figure 6. The surface contour of the surface profilometer structure 3.29. The vertical scale factor is 50.0 nm/division and the horizontal scale factor is approximately 10 μm/division. The A through G substructures are described in section 8.1.

The junction depths were obtained from the groove and stain method on unpatterned wafers included in the diffusion boat. The emitter junction depth, X_{je}, the base junction depth, X_{jb}, and the base width, X_{jbe}, are listed in table 3.

11. DISCUSSION

The primary purpose of this test pattern is to enable the evaluation of the resistivity-dopant density relation in both *n*- and *p*-type bulk silicon. This objective is currently being achieved by an ongoing program which uses test structures 3.8, 3.10, 3.17, and 3.26. The current status of this work is reviewed elsewhere [5]. Some other structures are used as diagnostic tools to verify that the structures of interest are fabricated properly. The remaining structures are experimental in nature and allow the exploration of new designs and measurement methods.

The novel designs developed in this test pattern include the piped-collector voltage taps which appear in structures 3.12, 3.17, and 3.18. This type of construction allows for the smallest contact area to bulk silicon while completely eliminating surface currents. The incorporation of a bulk Hall effect resistor (3.26) with other planar test structures is a novel feature of this test pattern, and this required the omission of the scribe avenues from the BASE and EMITTER masks. This omission does not hinder the scribing and breaking of wafers into chips. The combination of sheet resistance measurements from bridge (3.28) and van der Pauw (3.22) structures to obtain the effective base width is a new concept as is the orthogonal design of the van der Pauw structures (3.20, 3.21, and 3.22). This design is intended to be compatible with automatic pattern generators which draw only orthogonal lines. The incremental base sheet resistor (3.30) is an exploratory structure intended to assist in the automation of the incremental sheet resistance, anodic oxidation, dopant profile method. Its implementation awaits the development of a proper experimental apparatus. The incorporation of the surface profilometer structure (3.29) has proven invaluable especially in diagnosing fabrication problems with the collector four-probe resistor (3.17). Over-etch of the base-oxide islands was clearly visible in structure 3.29 (E) and (F). The modular arrangement of the five sheet and contact resistors (3.20, 3.21, 3.22, 3.23, 3.24) with four bonding pads arranged in a square is an attempt to assist the wafer probing of these structures. Other arrangements are possible; for example, the in-line pad array for structures 3.27 and 3.28; also see reference [1]. Optimum modular pad arrangements are being sought in conjunction with the design of various test structures.

ACKNOWLEDGEMENTS

The author wishes to thank all of the members of the Electronic Technology Division who have participated in both the fabrication and testing of the various test structures on this test pattern.

APPENDIX

In the following figures 7 through 10, the center-to-center distance between the scribe lines is 100 mils (2.54 mm).

Table 4 - Test Structures Shown in Figure 7

Number	Test Structure
3.1	Collector resistor (FP, CS)
3.2	MOS capacitor over base
3.3	MOS capacitor over emitter
3.4 N, P	Alignment markers
3.5	NBS logo
3.6	Tetrode transistor
3.7	Collector resistor (DGR)
3.8	MOS capacitor over collector (FP, CS)
3.9	Emitter-base diode (FP)
3.10	Base-collector diode (FP, CS)
3.11	Base sheet resistor (VDP, FP, CS)

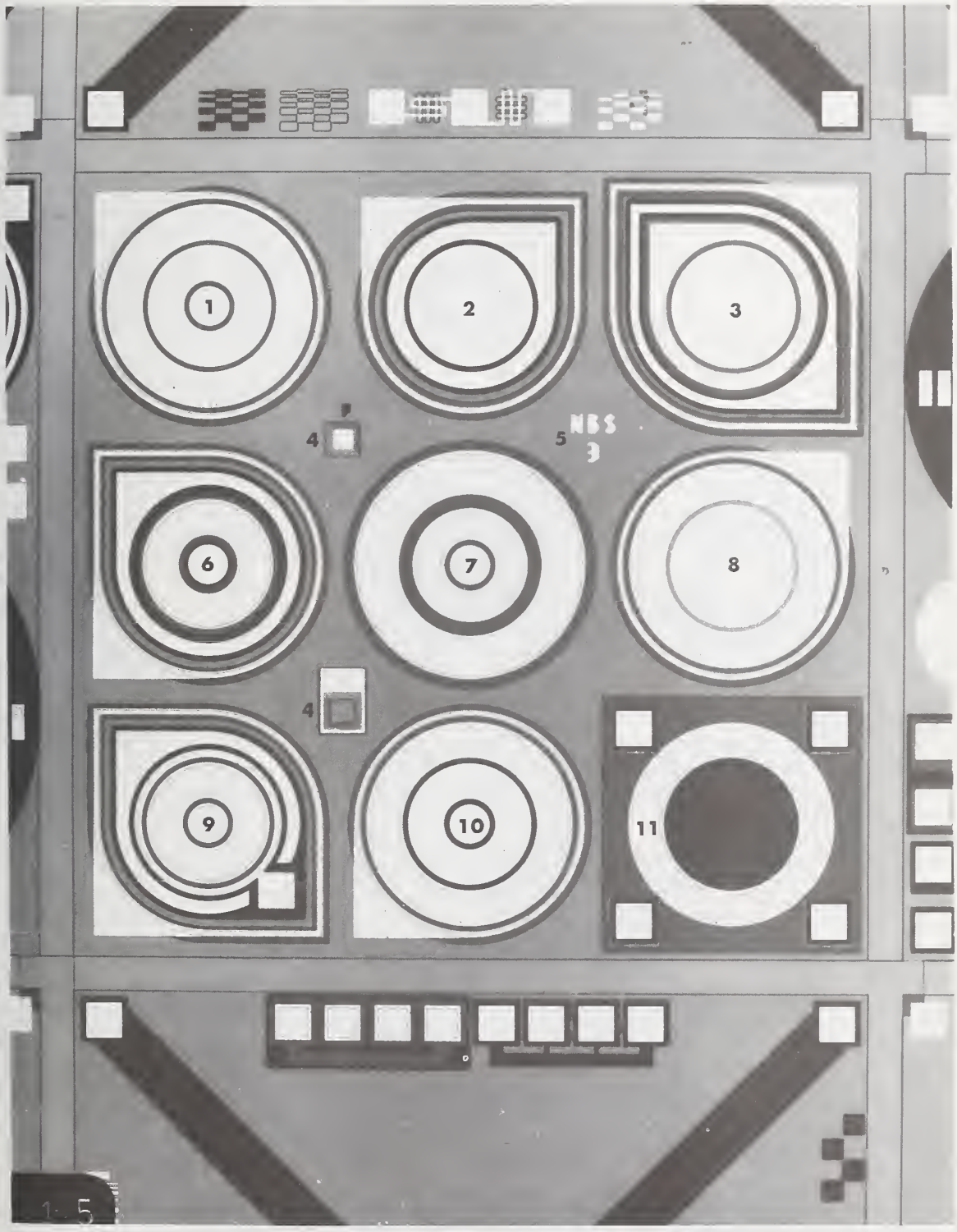


Figure 7. Test pattern NBS-3 quadrant 1.

Table 5 - Test Structures Shown in Figure 8

Number	Test Structure
3.12	Collector spreading resistor (small)
3.13	Bipolar transistor
3.14	Base-collector diode (FP, CS)
3.15	MOS transistor (circular)
3.16	MOS transistor
3.17	Collector four-probe resistor
3.18	Collector spreading resistor (large)
3.19	MOS capacitor over collector
3.20	Metal sheet resistor (VDP)
3.21	Emitter sheet resistor (VDP)
3.22	Base sheet resistor (VDP)
3.23	Metal-to-emitter contact resistor
3.24	Metal-to-base contact resistor
3.25	MOS capacitor over collector

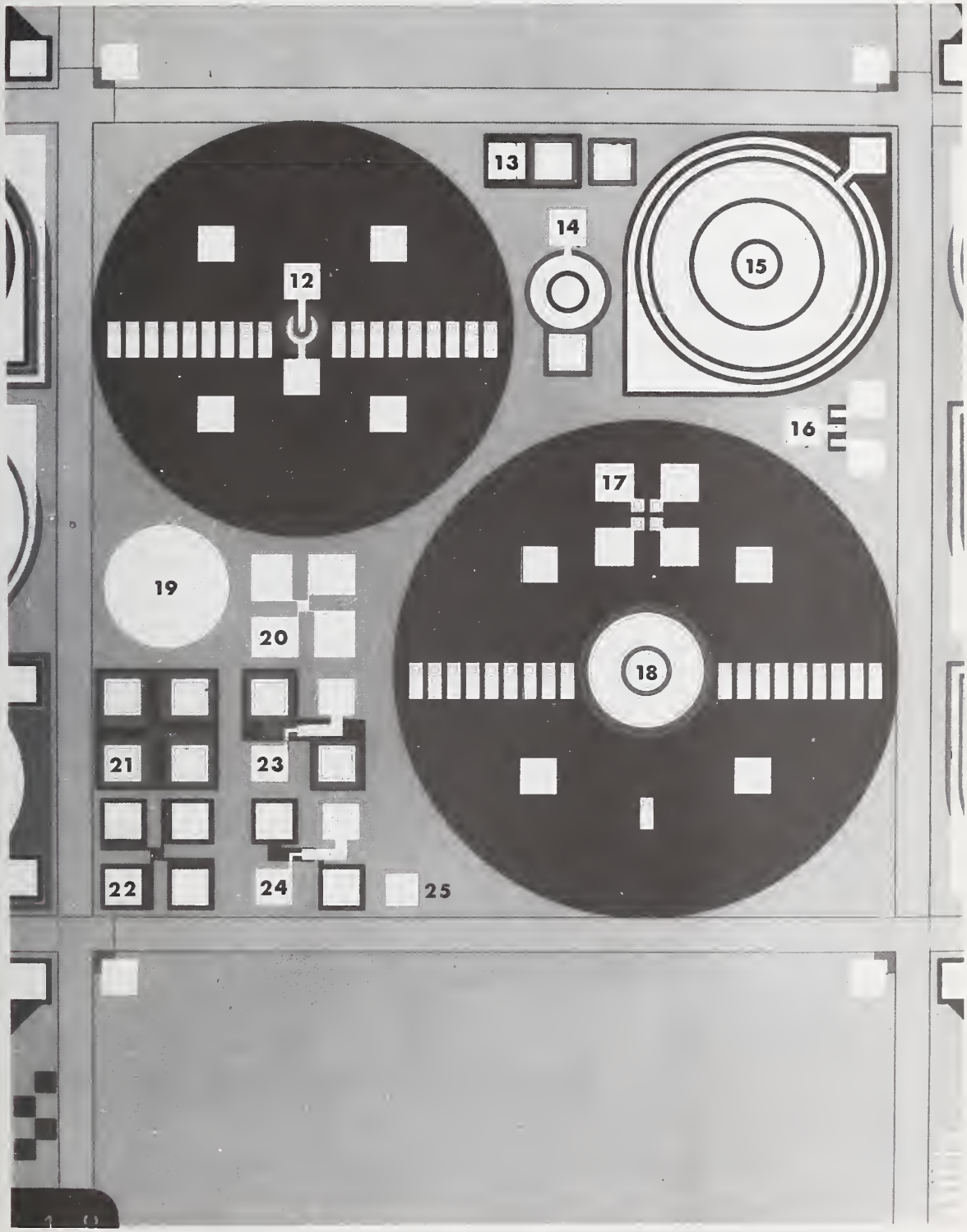


Figure 8. Test pattern NBS-3 quadrant 2.

Table 6. Test Structures Shown in Figure 9

Number	Test Structure
3.26	Collector Hall effect resistor

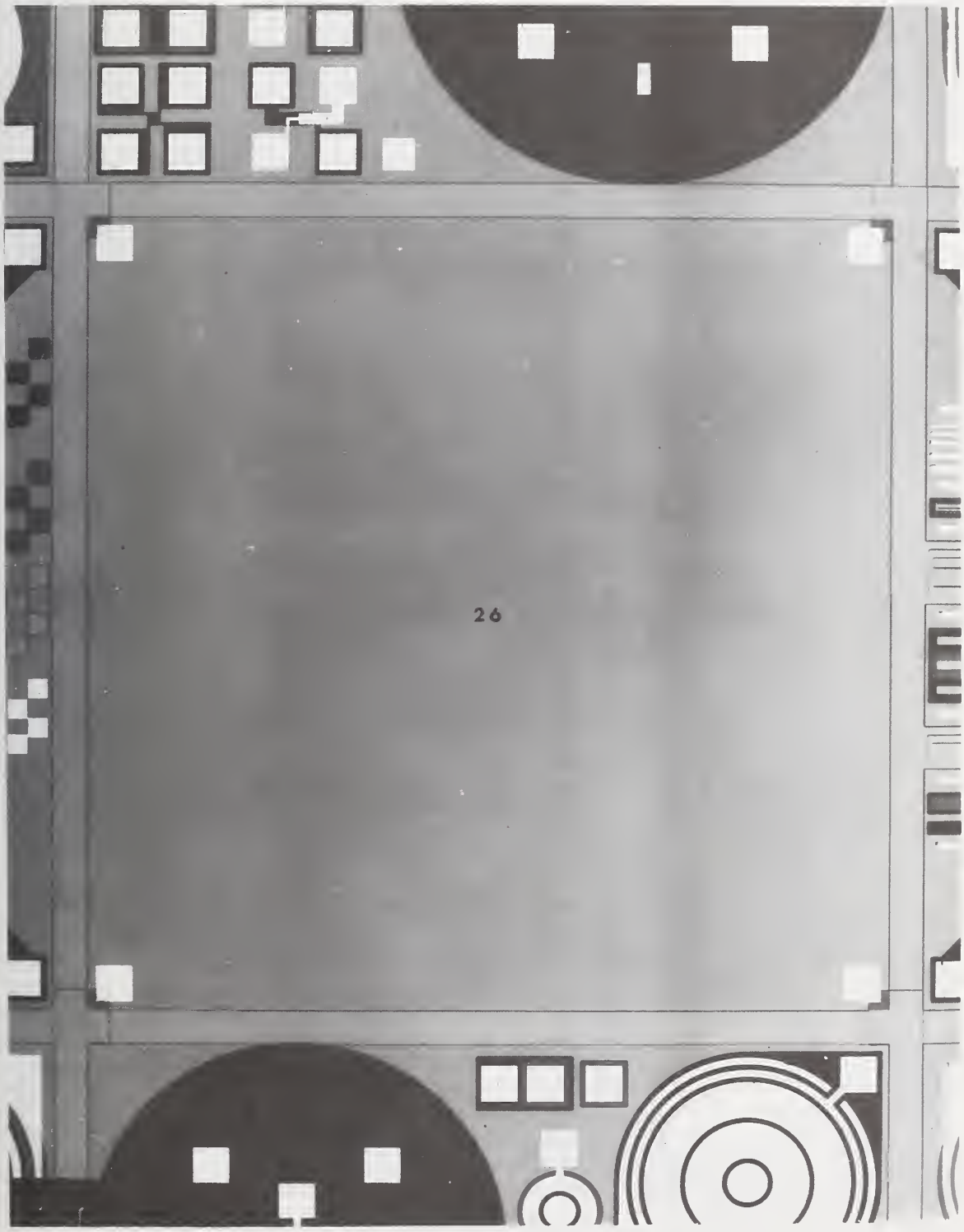


Figure 9. Test pattern NBS-3 quadrant 3.

Table 7. Test Structures Shown in Figure 10

Number	Test Structure
3.27	Emitter sheet resistor (B)
3.28	Base sheet resistor (B)
3.29	Surface profile structure
3.30	Incremental base sheet resistor (VDP)
3.31 B, E, C, M	Etch-control structures
3.32 B, C, M	Resolution structures
3.33	Metal step-coverage resistor

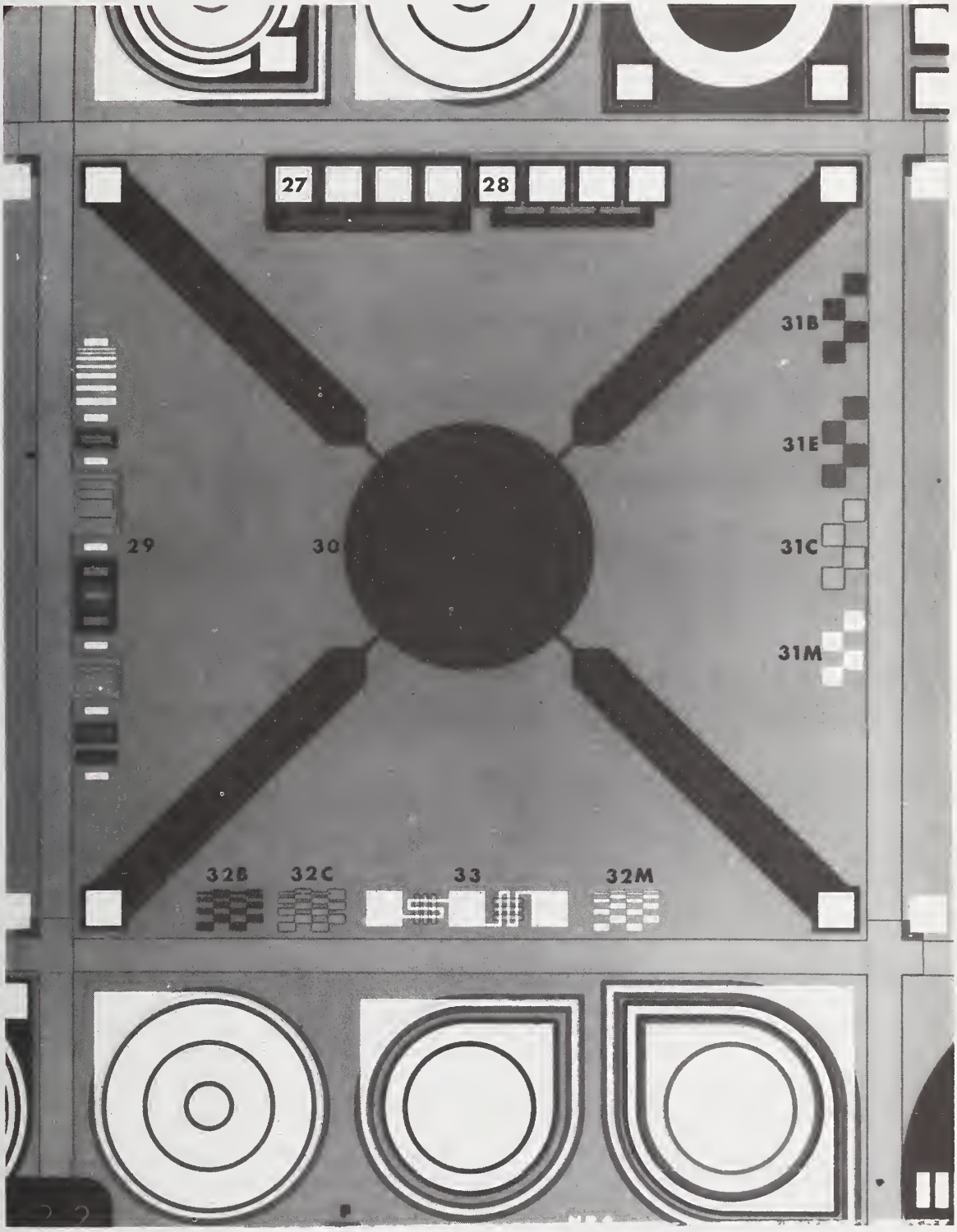


Figure 10. Test pattern NBS-3 quadrant 4.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

Test pattern NBS-3 is a microelectronic test vehicle designed by the National Bureau of Standards to evaluate the electronic materials used in discrete semiconductor devices and integrated circuits. Designed for fabrication on silicon wafers, the test pattern is an aid in better understanding integrated circuit fabrication technologies. The main pattern consists of four masks designated BASE, EMITTER, CONTACT, and METAL and contains 33 test structures such as sheet resistors, MOS capacitors, p-n junctions, bipolar and MOS transistors, and etch control and resolution structures.

The pattern was designed primarily to aid in the evaluation of the relationship between resistivity and dopant density in both n- and p-type silicon. This relation is needed in the design of silicon solid-state devices and in the analysis of various physical measurements. Other test structures are included for use as diagnostic tools to verify that proper fabrication procedures were followed. The remaining structures allow the exploration of new designs and measurement methods.

The structures are arranged in a square pattern 200 mil (5.08 mm) on a side. A detailed layout of each test structure is presented including both a top view and a cross sectional view. A description of each structure is given and where applicable the formulas for evaluating such quantities as resistivity, dopant density, and sheet resistance are given. The fabrication of the test pattern is illustrated by an n-p-n transistor process and values obtained from various test structures are presented.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Dopant density; microelectronics; MOS capacitors; n-p-n transistor fabrication; p-n junctions; resistivity; semiconductor electronics; sheet resistors; silicon; test pattern; test structures.

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